MOOGAMBIGAI CHARITABLE AND EDUCATIONAL TRUST

Rajarajeswari College of Engineering

(An Autonomous Institution under Visvesvaraya Technological University, Belagavi)
#14, Ramohalli Cross, Kumbalagodu, Mysore Road, Bengaluru–560074

Electronics and Communication Engineering

V & VI Semester Scheme and Syllabus

(2024 Scheme)

VISION

To empower young minds through technology, research and innovation, to produce technically competent and socially responsible professionals in higher education.

MISSION

1. To deliver excellence in education through innovative teaching, impactful research, and continuous skill development, preparing students to meet global challenges with technical expertise and ethical responsibility.
2. To foster a transformative learning environment that integrates technology, research and practical experience, empowering students to become skilled professionals and socially conscious leaders.
3. To cultivate a culture of lifelong learning and professional excellence by encouraging creativity, research, and community engagement, equipping students with the skills to thrive in a dynamic world.
4. To provide a holistic educational experience that combines advanced technology, hands-on research, and community-focused learning, shaping students into competent, ethical professionals who contribute positively to society.

QUALITY POLICY

Rajarajeswari College of Engineering is committed to imparting quality technical education that nurtures competent, ethical professionals with global relevance. We ensure academic excellence through a dynamic, outcome-based curriculum, experienced faculty, and cutting-edge infrastructure. Continuous improvement is driven by innovation, research and strong industry collaboration. We foster holistic development and a progressive environment that supports lifelong learning, teamwork, and professional growth.

CORE VALUES

Academic Excellence, Integrity, Innovation, Global Competence, Continuous Improvement.

Electronics and Communication Engineering

DEPARTMENT VISION

Actualize high Quality Electronics and Communication Engineering professionals showcasing Innovation, Research and Performance in the Frontier areas and capable of working local, global, environment contributing for Societal development through sustainable technology keeping high moral values.

DEPARTMENT MISSION

1. To give strong fundamental and contemporary knowledge to students with excellent curriculum and faculty.
2. Promoting Innovation and Research by creating ambiance by collaborating Industry & academics also involving them to do societal beneficial projects.
3. Imparting ethics to students through relevant practices.

PROGRAM OUTCOMES (POs)

PO1: Engineering Knowledge: Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization as specified in WK1 to WK4 respectively to develop to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development. (WK1 to WK4)

PO3: Design/Development of Solutions: Design creative solutions for complex engineering problems and design/develop systems /components / processes to meet identified needs with consideration for the public health and safety, whole-life cost, net zero carbon, culture, society and environment as required. (WK5)

PO4: Conduct Investigations of Complex Problems: Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modeling, analysis & interpretation of data to provide valid conclusions. (WK8).

PO5: Engineering Tool Usage: Create, select and apply appropriate techniques, resources and modern engineering & IT tools, including prediction and modeling recognizing their limitations to solve complex engineering problems. (WK2 and WK6)

PO6: The Engineer and The World: Analyze and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health, safety, legal framework, culture and environment. (WK1, WK5, WK7).

PO7: Ethics: Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national & international laws. (WK9)

PO8: Individual and Collaborative Team work: Function effectively as an individual, and as a member or leader in diverse/multi-disciplinary teams.

PO9: Communication: Communicate effectively and inclusively within the community and society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations considering cultural, language, and learning differences

PO10: Project Management and Finance: Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.

PO11: Life-Long Learning: Recognize the need for, and have the preparation and ability for i) independent and life-long learning ii) adaptability to new and emerging technologies and iii) critical thinking in the broadest context of technological change. (WK8)

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: Able to take up career in the Electronics & Communication industries to contribute by innovative design and products to help society.

PEO2: Capable to work in team with good communication skills, leadership qualities and ethics.

PEO3: Professional empowering by taking up higher education or updating knowledge in line with the changing trends of technology.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Demonstrate the competency to analyze the real time problems related to Electronics and communication industry and able to design and develop products with the cutting edge technology.

PSO2: Demonstrate leadership qualities to resolve the complex multidisciplinary engineering, societal challenges in the ethical manner.

INDEX

V Semester			
Sl. No.	**Course Code**	**Course Title**	**Page No.**
1.	B24EC501	Technological Innovation Management and Entrepreneurship	1
2.	B24EE502	Digital Signal Processing	4
3.	B24EC503	Communication System-II	7
4.	B24EC504	Embedded System Design	9
5.	B24EC505L	Digital Communication Lab	12
6.	B24EC561	Digital Image Processing	14
7.	B24EC562	Machine learning	16
8.	B24EC563	Analog CMOS Integrated Circuits	18
9.	B24EC564	Industry 4.0 and IoT	20
10.	B24EC581	Embedded System Design Lab	22
11.	B24EC582	Digital Image Processing Lab	24
12.	B24EC583	Measurement and Controls Lab	26
13.	B24EC584	Industry 4.0 and IoT lab	28
14.	B24ECP511	Miniproject	30

VI Semester			
Sl. No.	**Course Code**	**Course Title**	**Page No.**
1.	B24EC601	VLSI Design	32
2.	B24EC602	Data Communication Networks	34
3.	B24 EC631	Multimedia Communication	37
4.	B24EC632	Neural Networks	39
5.	B24EC633	RTOS(Real Time Operating Systems)	41
6.	B24EC634	Digital Circuit Design using Verilog	43
7.	B24EC641	Digital Electronics for Engineers	45
8.	B24EC642	Basics of VLSI Design	47
9.	B24EC643	Communication systems	49
10.	B24EC644	Electronics in Agricultural System	51
11.	B24EC605L	VLSI Design Lab	53
12.	B24EC681	Verilog HDL Lab	56
13.	B24EC682	System Modeling using Simulink Lab	58
14.	B24EC683	Machine Learning with Python Lab	60
15.	B24EC684	Fiber Optics Communication Lab	62

MOOGAMBIGAI CHARITABLE AND EDUCATIONAL TRUST

Rajarajeswari College of Engineering

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Scheme of Teaching and Examinations -2024 Scheme

Outcome based Education (OBE) and Choice Based Credit System (CBCS) Effective from the Academic Year 2026-27

V Semester

Sl. No	Course Category and Course Code		Course Title	TD / PSB	Teaching Hours / Week				Examination				Credits
					Lecture L	Tutorial T	Practical P	Self-Learning S	CIE Marks	SEE Duration in Hrs	SEE Marks	Total Marks	
1.	HSMC	B24EC501	Technological Innovation Management and Entrepreneurship	EC	3	0	0	3	50	3	50	100	3
2.	IPCC	B24EE502	Digital Signal Processing	EC	3	0	2	3	50	3	50	100	4
3.	PCC	B24EC503	Communication System-II	EC	2	2	0	2	50	3	50	100	3
4.	PCC	B24EC504	Embedded System Design	EC	3	0	0	3	50	3	50	100	3
5.	PCCL	B24EC505L	Digital Communication Lab	EC	0	0	2	0	50	3	50	100	1
6.	PEC	B24EC56X	Professional Elective Course- I	EC	3	0	0	3	50	3	50	100	3
7.	BSC	B24BEK507	Biology for Engineers	EC / Che	2	0	0	2	50	2	50	100	2
8.	AEC	B24EC58X	Ability Enhancement Course Lab - V	EC	0	0	2	0	50	3	50	100	1
9.	NCMC	B24NCK59X	NSS / NCC / PE / Yoga / Music	HSS	2	0	0	0	100	-	-	100	PP
10.	NCMC	B24ESK510	Environmental Science and E-Waste Management	EC / CV	2	0	0	0	100	-	-	100	PP
11.	SDC	B24ECP511	Mini Project	EC	0	0	4	0	50	3	50	100	2
								TOTAL	650		450	1100	22

BSC: Basic Science Course, HSMC: Humanity Social sciences including Management courses, IPCC: Integrated Professional Core Course, PCC: Professional Core Course, PCCL: Professional Core Course laboratory, NCMC: Non-Credit Mandatory Course, AEC: Ability Enhancement Course, PEC: Professional Elective Course, SDC- Skill Development Course, L: Lecture, T: Tutorial, P: Practical S: Self-Learning, CIE: Continuous Internal Evaluation, SEE: Semester End Evaluation. K: Indicates common course to all the streams of engineering, PP/NP: Pass/ Not Pass, YY: Programme Code (EC, CS, IS etc.,), X: 1/2/3/4.

Professional Elective Courses (PEC) - I			
B24EC561	Digital Image Processing	B24EC562	Machine learning
B24EC563	Analog CMOS Integrated Circuits	B24EC564	Industry 4.0 and IoT
Ability Enhancement Course / Skill Enhancement Course (AEC/SEC) – V			
B24EC581	Embedded System Design Lab	B24EC582	Digital Image Processing Lab
B24EC583	Measurement and Controls Lab	B24EC584	Industry 4.0 and IoT lab
Non-Credit Mandatory Courses (NCMC)			
B24NCK591	National Service Scheme	B24NCK592	National Cadet Corps
B24NCK593	Physical Education	B24NCK594	Yoga
B24NCK595	Music		

National Service Scheme/National Cadet Corps/Physical Education/Yoga/Music: All the students have to register the same course namely National Service Scheme (NSS), National Cadet Corps (NCC), Physical Education (PE), Yoga (YOG) and Music (MUS) during the first week of III/IV/V/VI semesters. However, the option is given to students to change the activity. He/she may opt for the change of the course in ensuing semester. If the student is opting new course in V semester first time, he/she may take the basic modules from the syllabus to complete and if they repeat the same course in ensuing semester, subsequent modules can be offered.

These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the course is mandatory for the award of degree.

Professional Elective Courses (PEC): A PEC is intended to enhance the depth and breadth of educational experience in the engineering and technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of student's strength for offering a professional elective is 10. However, this condition shall not be applicable to cases where the admission to the programme is less than 10 students.

HoD **Dean-Academics** **Principal**

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VI Semester

S. No	Course Category and Course Code		Course Title	TD / PSB	Teaching Hours / Week				Examination				Credits
					Lecture	Tutorial	Practical	Self-Learning	CIE Marks	SEE Duration Hrs	SEE Marks	Total Marks	
					L	T	P	S					
1.	PCC	B24EC601	VLSI Design	EC	2	2	0	2	50	3	50	100	3
2.	IPCC	B24EC602	Data Communication Networks	EC	3	0	2	3	50	3	50	100	4
3.	PEC	B24EC63X	Professional Elective Course- II	EC	3	0	0	3	50	3	50	100	3
4.	OEC	B24EC64X	Open Elective Course - I	Any Dept	3	0	0	3	50	3	50	100	3
5.	PCCL	B24EC605L	VLSI Design Lab	EC	0	0	2	0	50	3	50	100	1
6.	AEC	B24RMK606	Research Methodology and IPR	EC	1	0	0	1	50	2	50	100	1
7.	SDC	B24PRJ607	Capstone Project Work : Phase - I	EC	0	0	4	0	100	-	-	100	2
8.	AEC	B24EC68X	Ability Enhancement Course Lab – VI	EC	0	0	2	0	50	3	50	100	1
9.	NCMC	B24NCK69X	NSS / NCC / PE / Yoga / Music	HSS	2	0	0	0	100	-	-	100	PP
10.	HSMC	B24IKK610	Indian Knowledge System	EC	2	0	0	0	100	-	-	100	PP
								TOTAL	600		400	1000	18

HSMC: Humanity Social sciences including Management courses, IPCC: Integrated Professional Core Course, PCC: Professional Core Course, PCCL: Professional Core Course laboratory, NCMC: Non-Credit Mandatory Course, AEC: Ability Enhancement Course, PEC: Professional Elective Course, OEC: Open Elective Course, SDC- Skill Development Course, L: Lecture, T: Tutorial, P: Practical S: Self-Learning, CIE: Continuous Internal Evaluation, SEE: Semester End Evaluation. K: Indicates common course to all the streams of engineering, PP/NP: Pass/ Not Pass, YY: Programme Code (EC, CS, IS etc.,), X: 1/2/3/4

Professional Elective Courses (PEC) - II			
B24 EC631	Multimedia Communication	B24EC632	Neural Networks
B24EC633	RTOS(Real Time Operating Systems)	B24EC634	Digital Circuit Design using Verilog
Open Elective Course (OEC)- I			
B24EC641	Digital Electronics for Engineers	B24EC642	Basics of VLSI Design
B24EC643	Communication systems	B24EC644	Electronics in Agricultural System
Ability Enhancement Course (AEC) – VI			
B24EC681	Verilog HDL Lab	B24EC682	System Modeling using Simulink Lab
B24EC683	Machine Learning with Python Lab	B24EC684	Fiber Optics Communication Lab
Non-Credit Mandatory Courses (NCMC)			
B24NCK691	National Service Scheme	B24NCK692	National Cadet Corps
B24NCK693	Physical Education	B24NCK694	Yoga
B24NCK695	Music		

PROJECT WORK: **Phase – I:** The objective of the Project work is (i) To encourage independent learning and the innovative attitude of the students. (ii) To develop interactive attitude, communication skills, organization, time management, and presentation skills. (iii) To impart flexibility and adaptability. (iv) To inspire team working. (v) To expand intellectual capacity, credibility, judgment and intuition. (vi) To adhere to punctuality, setting and meeting deadlines. (vii) To install responsibilities to oneself and others. (viii)To train students to present the topic of project work in a seminar without any fear, face the audience confidently, enhance communication skills, involve in group discussion to present and exchange ideas.

CIE Procedure for Project Work: The CIE marks shall be awarded by a committee consisting of the Head of the concerned department and two senior faculty members of the department, one of whom shall be the Guide. The CIE marks awarded for the project work shall be based on the evaluation of the **Project Work Report, Project Reviews and Viva-Voce.** The marks awarded for the project report shall be the same for all the batch mates.

SEE procedure for Project Work: SEE for project work will be conducted by the two examiners appointed by the Institution. The SEE marks awarded for the project work shall be based on the evaluation of **Project Demonstration, Project Presentation and Viva-Voce** in the ratio 20:60:20.

Open Elective Courses: Students belonging to a particular stream of Engineering are not entitled to the open electives offered by their parent department. However, they can opt for an elective offered by other departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Mentor. The minimum number of students' for offering Open Elective Course is 10. However, this condition shall not be applicable to class where the admission to the program is less than 10.

HoD **Dean-Academics** **Principal**

Semester-V					
Technological Innovation Management and Entrepreneurship **Category: HSMC** **(Common to ECE & EEE)**					
Course Code	:	**B24EC501**	CIE	:	50 Marks
Teaching Hours L:T :P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To understand basic skills of Management.
2.	To understand the need for Entrepreneurs and their skills.
3.	To identify the Management functions and Social responsibilities.
4.	To understand economic development, creativity and Innovation.
5.	To understand the Ideation Process, creation of Business Model, Feasibility Study and sources of funding.

Module – 1	**No. of Hours**
Management: Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession. **Planning:** Planning-Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making.	9
Module – 2	**No. of Hours**
Organizing: Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalization, Committees–Meaning, Types of Committees; Centralization Vs Decentralization of Authority and Responsibility; **Staffing**-Need and Importance**,** Recruitment and Selection Process. **Directing and Controlling:** Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication –Meaning, Importance and Purposes of Communication; Leadership-Meaning, Characteristics, Behavioral Approach of Leadership; Coordination-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process.	9
Module – 3	**No. of Hours**
Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance. **Entrepreneurship**: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur ,Classification of Entrepreneurs, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship **.**	9
Module - 4	**No. of Hours**
Modern Small Business Enterprises: Role of Small Scale Industries, Impact of Globalization and WTO on SSIs, Concepts and definitions of SSI Enterprises, Government policy and development of the Small Scale sector in India, Growth and Performance of Small Scale Industries in India, Sickness in SSI sector, Problems for Small Scale Industries, Ancillary Industry and Tiny Industry (Definition only). **Idea Generation and Feasibility Analysis-** Idea Generation; Creativity and Innovation; Identification of Business Opportunities; Market Entry Strategies; Marketing Feasibility; Financial Feasibilities; Political Feasibilities; Economic Feasibility; Social and Legal Feasibilities; Technical Feasibilities; Managerial Feasibility, Location and Other Utilities Feasibilities.	9
Module – 5	**No. of Hours**
Business Model & Business Plan: Meaning and importance of business models, Scope and need of a business plan, Financial, Marketing, HR, and Production/Service plans, Formats of business plans (traditional vs. pitch deck),Reasons why business plans fail. **Financing Model:** Advanced methods of financial opportunity identification and evaluation Comparative analysis of banking and non-banking financing sources. Role of development financial	9

institutions and support agencies in entrepreneurship. Venture Capital**:** stages of funding, risk assessment, and entrepreneur–investor relationship. Evaluation of government funding schemes for startups and MSMEs. Financial planning for pre-launch, launch, and post-launch stages. Legal and procedural aspects of business licensing and registration. Critical analysis of challenges and difficulties in starting an enterprise. Case-based study on startup financing failures and success factors.	

Course Outcomes: At the end of the course, the students will be able to	
CO1	Understand the fundamental concepts of Management and Entrepreneurship and opportunities in order to setup a business.
CO2	Describe the functions of Managers, Entrepreneurs and their social responsibilities.
CO3	Understand the components in developing a business plan, along with the integration of CSR-Corporate Social Responsibility.
CO4	Describe the importance of small scale industries in economic development and institutional support to start a small scale industry and understand the concepts of Creativity and Innovation and Identification of Business Opportunities.
CO5	Understand about various sources of funding and institutions supporting entrepreneurs.

Text Books	
1.	Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
2.	Dynamics of Entrepreneurial Development and Management by Vasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.

Reference Text Books	
1.	Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.
2.	Robert D. Hisrich, Mathew J. Manimala, Michael P Peters and Dean A. Shepherd, "Entrepreneurship", 8th Edition, Tata Mc-graw Hill Publishing Co.ltd.-new Delhi, 2012.
3.	Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, Pearson Education 2008, ISBN 978-81-7758-260-4.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.

4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	1	-	-	-	3	1	-	-	1	1
CO2	2	2	-	-	-	2	1	-	-	2	1
CO3	1	1	-	-	-	1	2	-	-	2	1
CO4	1	1	-	-	-	1	2	-	-	1	1
CO5	1	1	-	-	-	1	2	-	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-V					
Digital Signal Processing **Category: IPCC**					
Course Code	:	**B24EE502**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:2:3	SEE	:	50 Marks
Total Hours	:	45+30	Total	:	100 Marks
Credits	:	4	SEE Duration	:	3 Hrs

Course Learning Objective is to	
1.	Understand the classification, properties and basic operations of continuous-time and discrete-time signals and systems.
2.	Analyze Linear Time-Invariant systems using impulse response, convolution integral and convolution sum.
3.	Apply Z-Transform and Discrete-Time Fourier Transform for analysis of discrete-time signals and LTI systems.
4.	Understand DFT and FFT algorithms for efficient frequency-domain analysis of discrete-time signals.
5.	Design and realize IIR and FIR digital filters using standard design techniques and structures.

Module – 1	**No. of Hours**
Signals and System: Introduction to signals and system, classification of signals, basic operations on signals, Elementary signals, and properties of systems. **LTI Systems**: Time-Domain Representations, impulse response, Time domain Convolution (Integral and Sum), and properties.	9
Module – 2	**No. of Hours**
Z-Transforms: Introduction, Z-transform, properties of the Region of Convergence, properties of the Z-Transform, Inversion of the Z-Transform, transform analysis of LTI systems, solution of difference equations. **Discrete-Time Fourier Transform (DTFT)**: Introduction, properties of DTFT, frequency response of LTI system.	9
Module – 3	**No. of Hours**
Discrete Fourier Transform (DFT): Frequency domain sampling, Properties of DFT, Linear convolution using DFT. **Fast-Fourier-Transform (FFT) Algorithms**: Direct computation of DFT, need for efficient computation of the DFT using FFT algorithms, Radix-2 FFT algorithms for the computation of DFT and IDFT based on Decimation-in-Time (DIT) and Decimation-in-Frequency (DIF) algorithms.	9
Module – 4	**No. of Hours**
Infinite Impulse Response (IIR) Filters: Analog Butterworth and Chebyshev filter design. Develop IIR filters using Impulse Invariance Method, and Bilinear Transformation Methods. **IIR filter Structures:** Direct forms, Cascade form and parallel form.	9
Module – 5	**No. of Hours**
Finite Impulse Response (FIR) Filters: FIR filter design by window techniques and frequency sampling techniques. **Structures of FIR Filters:** Direct form, Cascade form and linear phase structures.	9

LABORATORY

Practical Component of IPCC (12 Experiments using MATLAB)

Sl. No.	Name of the Experiments
1	Programs to generate the following discrete time signals: a) Unit sample sequence b) Unit step sequence c) Exponential sequence d) Sinusoidal sequence e) Random sequence
2	Program to perform the following operations on signals: a) Signal addition b) Signal multiplication c) Scaling d) Shifting e) Folding
3	Program to perform convolution of two given sequences with and without using built-in function. Display the result.
4	Evaluation of impulse response of a system. Plot the magnitude and phase spectrum.
5	Computation of N-point DFT of a given sequence with and without using built-in function. Plot the magnitude and phase spectrum.
6	Using the DFT and IDFT, compute the following for any two given sequences: a) Circular convolution b) Linear convolution
7	Determine ZT, plot poles and zeros. Analyze stability of DT Systems
8	Develop decimation-in-time radix-2 FFT algorithm with and without using built-in functions.
9	Design and implementation of IIR filters using Impulse Invariance Method to meet the given specifications.
10	Design and implementation of IIR filters Bilinear Transformation Method to meet the given specifications.
11	Design and implementation of FIR filters using window technique to meet the given specifications.
12	Design and implementation of FIR filters using frequency sampling method to meet the given specifications.

Course Outcomes: At the end of the course, the students will be able to	
CO1	Classify and analyze continuous-time and discrete-time signals and systems using standard signal operations and system properties.
CO2	Determine the time-domain response of Linear Time-Invariant systems using impulse response, convolution integral and convolution sum.
CO3	Apply Z-Transform and Discrete-Time Fourier Transform techniques to analyze discrete-time signals, LTI systems and solve difference equations.
CO4	Compute DFT and FFT for frequency-domain analysis of discrete-time signals and evaluate linear convolution using DFT.
CO5	Design and realize IIR and FIR digital filters using standard transformation, windowing, frequency sampling and structural realization techniques.

Text Books	
1.	Simon Haykins & Barry Van Veen, "Signals & Systems", 2nd edition, John Wiley & Sons, 2002.
2.	Proakis & Monalakis, "Digital Signal Processing - Principles Algorithms and Applications", 4th Edition, Pearson education, 2009.

Reference Text Books	
1.	Digital Signal Processing, A. NagoorKani, McGraw Hill, 2nd Edition, 2012.
2.	Digital Signal Processing, Shaila D. Apte, Wiley, 2nd Edition, 2009.
3.	Digital Signal Processing, Ashok Amberdar, Cengage, 1st Edition, 2007.
4.	Digital Signal Processing, Tarun Kumar Rawat, Oxford, 1st Edition, 2015.

Web links and Video lectures (e-Resources):
1. http://www.freebookcentre.net/Electronics/DSP-Books
2. https://www.electronicsforu.com/special/cool-stuff-misc/8-free-digital-signal-processing-ebooks

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the

academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**30** (Average of Best Two Assessments)	**50/2 = 25**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	Any One Assessments as per regulations	**20**	**20**	
Laboratory	**Lab conduction & Record**	Evaluating each expt. for 10 marks.	**05**	**25**
	Internal Test	**50**	**20**	
Total Marks				**50**
SEE	**Semester End Examination**	**100**	**50**	**50**
Total marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice. Students should answer five full questions, selecting one full question from each module.
5. Students have to answer for 100 marks and marks scored out of 100 shall be proportionally reduced to 50 marks.
6. The maximum marks from the practical component to be included in the SEE question paper is **16 marks.**
7. Question papers to be set as per the Blooms Taxonomy levels.
8. The laboratory component of the **integrated course** shall be CIE only. However, in SEE, the questions from the practical component shall be included.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	-	1	1	-	-	-	-	1	-
CO2	3	3	1	2	1	-	-	-	-	1	-
CO3	3	3	1	2	2	-	-	-	-	1	-
CO4	3	3	2	2	3	-	-	-	-	1	-
CO5	3	3	3	2	3	-	-	-	1	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester -V					
Communication System-II **Category: PCC**					
Course Code	:	**B24EC503**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	2:2:0:2	SEE	:	50 Marks
Total Hours	:	55	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.
2.	To Learn the different digital modulation techniques.
3.	To Understand the idea of information theory.
4.	To Understand the basic principles of information theory and various source coding techniques.
5.	To Understand the concepts of convolution codes and analyze the code words using time domain and transform domain approach.

Module – 1	**No. of Hours**
Bandpass Signals to Equivalent Lowpass: Hilbert Transform, Pre-envelopes, Complex envelopes of Band-pass Signals, Canonical Representation of Bandpass signals. **Signaling over AWGN Channels:** Introduction, Geometric representation of signals, Gram- Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel , Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver.	11
Module – 2	**No. of Hours**
Digital Modulation Techniques: Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M–ary PSK, M–ary QAM. Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability. BFSK using Non coherent Detection, Differential Phase Shift Keying.	11
Module – 3	**No. of Hours**
Information theory: Introduction, Entropy, Source Coding Theorem, Lossless Data Compression Algorithms, Discrete Memory less Channels, Mutual Information, Channel capacity, Channel Coding Theorem , Information Capacity Law (Statement).	11
Module – 4	**No. of Hours**
Error Control Coding: Error Control Using Forward error Correction, **Linear Block Codes:** Definitions, Matrix Descriptions, Syndrome and its properties, Minimum distance Considerations, Syndrome Decoding, Hamming Codes. **Cyclic Codes**: Properties, Generator and Parity Check Polynomial and matrices, Encoding, Syndrome computation, Examples	11
Module – 5	**No. of Hours**
Convolution Codes: Convolution Encoder, Code tree, Trellis Graph and State graph, Recursive systematic Convolution codes, Optimum decoding of Convolution codes, Maximum Likelihood Decoding of Convolution codes: The Viterbi Algorithm, Examples.	11

Course Outcomes: At the end of the course, the students will be able to	
CO1	Apply the concept of signal conversion to vectors in communication transmission and reception.
CO2	Analyze the different coherent and non-coherent digital modulation techniques.
CO3	Analyze entropy and source coding techniques.
CO4	Apply the Source coding and Channel coding principles for the discrete memory less channels and Compute the code words for using Linear Block Code.
CO5	Design encoding and decoding circuits for Cyclic Codes and Convolution Codes.

Text Books	
1.	Simon Haykin, “Digital Communication Systems”, John Wiley & sons, 2014, ISBN 978-81- 265-4231-4.
2.	K.N HariBhat, D. Ganesh Rao, “Information Theory and Coding”, Cengage Learning India Pvt Ltd, 2017, ISBN: 93-866-5092-4,

Reference Text Books	
1.	B.P Lathi, Zhi Ding, "Modern Digital and Analog Communication Systems",4th Edition, Oxford University press, ISBN: 9780198073802, 2017
2.	K Sam Shanmugam, "Digital and analog communication systems", Wiley India Pvt. Ltd, 2017, ISBN: 978- 81-265-3680-1,.

Web links and Video lectures (e-Resources)
1. Principles of Communication Systems Part II, https://onlinecourses.nptel.ac.in/noc19_ee47/preview

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and it carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	2	-	2	1	-	-	-	-	-	1
CO2	2	1	-	-	1	-	-	-	-	-	1
CO3	3	1	-	2	1	-	-	-	-	-	1
CO4	3	1	-	2	1	-	-	-	-	-	1
CO5	3	1	-	2	-	-	-	-	-	-	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-V					
Embedded System Design **Category: PCC**					
Course Code	:	**B24EC504**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To Identify various components, their purpose, and their application to the embedded system's applicability.
2.	To Understand to design, analyze, and optimize embedded systems through integrated hardware and software co-design methodologies for efficient and reliable system performance
3.	To Understand the embedded system's real-time operating system and its application in IoT.
4.	To Understand the fundamentals of ARM-based systems, including architecture and its units likeregisters , debug interface, stack, MPU, Interrupts etc.
5.	To Use the various instructions to program the ARM controller.

Module– 1	**No.of Hrs**
Introduction to Embedded System: What is an Embedded Systems? Embedded systems Vs General computing systems, History of Embedded Systems, Classification of Embedded systems, Purpose of Embedded Systems, The Typical Embedded System, Microprocessor v/s Microcontroller, Differences between RISC and CISC, Harvard v/s Von- Neumann Processor/Controller Architecture, Big-endian V/s Little-endian processors **Embedded System Design Concepts:** Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific	9
Module– 2	**No.of Hrs**
Hardware Software Co-Design: Embedded firmware design approaches, computational models, embeddedfirmware development languages, Integration and testing of Embedded Hardware and firmware, Components inembedded system development environment(IDE),Files generated during compilation, simulators, emulators and debugging.	9
Module– 3	**No.of Hrs**
Operating System Basics: Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock. How to choose an RTOS, Integration and testing of Embedded hardware and firmware	9
Module– 4	**No.of Hrs**
Introduction, RISC design philosophy: ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. ARM Processor Fundamentals, ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions	9
Module– 5	**No.of Hrs**
ARM Instruction Set: nIntroduction, Data processing instructions, Load – Store instruction, Software interrupt instructions, Program status register instructions, Loading constants,ARMv5E extensions, Conditional Execution. **C Compilers and Optimization:** Basic C Data Types, C Looping Structures, Register Allocation, Function Calls, Pointer Aliasing	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Identify the various components of an embedded system, explain their purpose, and analyze their applicability in real-world embedded system applications
CO2	Understand the fundamental concepts and design flow of hardware–software co-design in embedde systems.
CO3	Explain the concepts of real-time operating systems (RTOS) used in embedded systems and analyze their applications in Internet of Things (IoT) systems

CO4	Express the fundamentals of ARM-based systems, including ARM architecture and core units such as registers, stack, memory protection unit (MPU), interrupt handling, and debug interfaces.
CO5	Apply ARM instruction sets to develop, program, and debug applications using ARM-based controllers.

Text Books	
1.	Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education, 2016
2.	Andrew N Sloss, Dominic System and Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publisher, 1st Edition, 2008.
3.	Peckol, "Embedded System Design", John Wiley & Sons, 2010.

Reference Text Books	
1.	Raj Kamal, "Embedded Systems: Architecture and Programming", Tata McGraw Hill, 2008.
2.	Tammy Noergaard, "Embedded System Architecture, A comprehensive Guide for Engineers and Programmers", Elsevier, 2006
3.	Lyla B Das," Embedded Systems-An Integrated Approach", Pearson2013

Web links and Video lectures (e-Resources)
1. https://archive.nptel.ac.in/courses/106/105/106105193/
2. https://developer.arm.com/documentation/dui0068/b/ARM-Instruction-Reference
3. https://www.udemy.com/course/introduction-to-arm-cortex-m3-and-m4-processors/
4. www.Nuvoton .com/websites on Advanced ARM Cortex Processors
5. https://alison.com/tag/embedded-systems

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	Internal Assessment-1	50	30 (Average of Best two Assessments)	50
	Internal Assessment-2	50		
	Internal Assessment-3	50		
AAT	Two Assessments as per regulations	20	20	
SEE	Semester End Examination	100	50	50
Total Marks				100

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	3	3	1	3	-	-	-	-	3	1
CO2	3	3	3	1	3	-	-	-	-	2	1
CO3	3	3	3	1	3	-	-	-	-	2	1
CO4	3	3	3	1	3	-	-	-	-	2	1
CO5	3	3	3	1	3	-	-	-	-	2	1

Level 3- High, Level 2- Moderate, Level 1-Low

Semester-V					
Digital Communication Lab **Category: PCCL**					
Course Code	:	**B24EC505L**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	0:0:2:0	SEE	:	50 Marks
Total Hours	:	30	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To design of basic digital modulation techniques using electronic hardware.
2.	To simulation of vector computations and derive the orthonormal basis set using Gram Schmidt procedure.
3.	To simulate the digital transmission and reception in AWGN channe.
4.	To simulate the digital modulations using software and display the signals and its vector representations.
5.	To implement the source coding algorithms using a suitable software platform

Sl. No	**List of Experiments**
1.	Generation and demodulation of the Amplitude Shift Keying signal.
2.	Generation and demodulation of the Binary Phase Shift Keying signal.
3.	Generation and demodulation of the Frequency Shift Keying signal.
4.	Generation of DPSK signal and detection of data using DPSK transmitter and receiver.
5.	Gram-Schmidt Orthogonalization: To find orthogonal basis vectors for the given setof vectors and plot the orthonormal vectors.
6.	Simulation of binary baseband signals using a rectangular pulse and estimate the BER for AWGN channel using matched filter receiver.
7.	Perform the QPSK Modulation and demodulation. Display the signal and its constellation.
8.	Generate 16-QAM Modulation and obtain the QAM constellation.
9.	Encoding and Decoding of Huffman code.
10.	Encoding and Decoding of binary data using a Hamming code.
11.	For a given data, use CRC-CCITT polynomial to obtain the CRC code. Verify for the cases, a) Without error b) With error.
12.	Encoding and Decoding of Convolution code

Course Outcomes: At the end of the course, the students will be able to	
CO1	Design the basic digital modulation and demodulation circuits for different engineering applications.
CO2	Design of optimum communication receivers for AWGN channels
CO3	Illustration of different digital modulations using the signals and its equivalent vector representations.
CO4	Implement the source coding and channel coding procedures using suitable software.
CO5	Design of Encoding and Decoding of Huffman and Hamming code.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Laboratory	**Lab Conduction & Record**	**Evaluating each expt. for 10 marks**	**20**	**50**
	Laboratory Test -1	**50**	**15**	
	Laboratory Test -2	**50**	**15**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
4. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
5. Change of experiment is allowed only once and 15% of Marks allotted to the Conduction procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	2	3	1	2	-	-	-	-	-	1
CO2	2	2	3	1	2	-	-	-	-	-	1
CO3	2	2	3	1	2	-	-	-	-	-	1
CO4	2	1	3	1	2	-	-	-	-	-	1
CO5	2	1	3	1	2	-	-	-	-	-	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-V					
Digital Image Processing **Category: PEC-I**					
Course Code	:	**B24EC561**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To understand the fundamentals of digital image processing.
2.	To understand the image transform used in digital image processing.
3.	To understand the image enhancement techniques in spatial domain used in digital image processing.
4.	To understand the Color Image Processing and frequency domain enhancement techniques in digital image processing.
5.	To understand the image restoration techniques and methods used in digital image processing.

Module – 1	**No. of Hours**
Digital Image Fundamentals: What is Digital Image Processing? Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels.	9
Module – 2	**No. of Hours**
Image Transforms: Introduction, Two-Dimensional Orthogonal and Unitary Transforms, Properties of Unitary Transforms, Two-Dimensional DFT, cosine Transform, Haar Transform.	9
Module – 3	**No. of Hours**
Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters	9
Module – 4	**No. of Hours**
Frequency Domain: Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters. Color Image Processing: Color Fundamentals, Color Models, Pseudo-color Image Processing.	9
Module – 5	**No. of Hours**
Image Segmentation: Introduction, Detection of isolated points, line detection, Edge detection, Edge linking, Region based segmentation- Region growing, split and merge technique, local processing, regional processing, Hough transform, Segmentation using Threshold.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Analyze image formation and the role of human visual system plays in the perception of gray and color image data.
CO2	Compute various transforms on digital images.
CO3	Conduct an independent study and analysis of Image Enhancement techniques.
CO4	Apply image processing techniques in the frequency (Fourier) domain.
CO5	Apply image processing techniques for segmentation.

Text Books	
1.	Digital Image Processing- Rafael C Gonzalez and Richard E Woods, PHI, 3rd Edition 2010.
2.	Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014.

Reference Text Books	
1.	Digital Image Processing- S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2014.
2.	Milan Sonka,"Image Processing, analysis and Machine Vision", Thomson Press India Ltd, 4th Edition.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	-	1	-	-	-	2	1	-	-	-	2
CO2	1	2	-	-	-	2	1	-	-	-	2
CO3	1	1	-	-	-	2	2	-	-	1	1
CO4	1	2	-	-	-	1	2	-	-	1	1
CO5	1	2	-	-	-	1	2	-	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-V					
Machine Learning Category **PEC-I**					
Course Code	:	**B24EC562**	CIE	:	50 Marks
Teaching Hours L : T : P : S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3Hrs

Course Laerning Objective is	
1.	To understand the fundamentals of Machine Learning and its types**.**
2.	To apply regression techniques for prediction and data analysis.
3.	To apply classification algorithms and model evaluation metrics for engineering problems.
4.	To apply ensemble learning, clustering and cluster evaluation methods.
5.	To understand Artificial Neural Networks and Reinforcement Learning for intelligent applications.

Module– 1	**No. of Hours**
Overview of Machine Learning: Need for Machine Learning, Machine Learning and Artificial Intelligence, Machine Learning and Statistics, Types of Machine Learning, Supervised Learning and Unsupervised Learning, semi-supervised Learning, Reinforcement Learning, Challenges of Machine Learning, Machine Learning Process, Machine Learning Applications.	9
Module– 2	**No. of Hours**
Regression Analysis: Introduction to Regression, Introduction to Linearity, Correlation, and Causation, Validation of Regression Methods, Multiple Linear Regression, Polynomial Regression, Logistic Regression, Ridge Regularization, LASSO, and Elastic Net.	9
Module– 3	**No. of Hours**
Support Vector Machines: Introduction to Support Vector Machines, Optimal Hyperplane, K-Nearest Neighbors(KNN), **Bayesian Learning:** Classification using Bayes Model-Naïve Bayes Algorithm, Brute Force Bayes Algorithm , Bayes Optimal Classifier, Gibbs Algorithm, Model Evaluation Metrics	9
Module– 4	**No. of Hours**
Ensemble Learning: Introduction, Parallel Ensemble Models – Random Forest. **Clustering Algorithms:** Introduction to Clustering Algorithms, Proximity Measures, Partitional Clustering Algorithm, Density based Methods, Cluster Evaluation Methods.	9
Module– 5	**No. of Hours**
Artificial Neural Networks: Introduction, Biological Neurons, Artificial Neurons, Simple Model of an Artificial Neuron, Artificial Neural Network Structure, Activation Functions. Types of ANN: Feed forward, Feedback. **Reinforcement Learning:** Overview of Reinforcement Learning, Scope of Reinforcement Learning, Reinforcement Learning As Machine Learning, Components of Reinforcement Learning, Markov Decision Process , Q-Learning.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Understand the foundational concepts, algorithms and methodologies of machine learning.
CO2	Apply variety of machine learning algorithms to solve engineering problems.
CO3	Evaluate machine learning models using suitable performance metrics.
CO4	Apply ensemble learning and clustering to analyze data.
CO5	Implement basic Artificial Neural Networks and Reinforcement Learning techniques.

Text Books	
1.	Machine Learning S. Sridhar and M. Vijayalakshmi, *Machine Learning*, 1st Edition, Oxford University Press, 2021.

Reference Text Books	
1.	Tom M. Mitchell, *Machine Learning*, McGraw-Hill, 1997.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	Internal Assessment-1	50	30 (Average of Best two Assessments)	50
	Internal Assessment-2	50		
	Internal Assessment-3	50		
AAT	Two Assessments as per regulations	20	20	
SEE	Semester End Examination	100	50	50
Total Marks				100

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	1	1	1	-	-	-	-	-	-	-	1
CO2	2	2	1	-	-	2	-	-	-	-	2
CO3	2	2	1	-	-	2	-	-	-	-	2
CO4	2	2	1	-	-	2	-	-	-	-	2
CO5	2	2	1	-	-	2	-	-	-	-	2

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-V					
Analog CMOS Integrated Circuits **Category: PEC-I**					
Course Code	:	**B24EC563**	CIE	:	50 Marks
Teaching Hours L:T :P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To study the basic MOS device physics.
2.	To study the analysis of single stage common source and common drain MOS amplifiers.
3.	To study the analysis of single stage common gate MOS amplifiers.
4.	To study the design of differential amplifiers.
5.	To study the operation of active and passive current mirrors.

Module – 1	**No. of Hours**
Basic MOS Device Physics: General considerations, MOS I/V characteristics, Second order effects, MOS device models – MOS device capacitances, small signal model.	9
Module – 2	**No. of Hours**
Single stage amplifiers: Common source stage with resistive load, Diode-connected load, current-source load, triode load, source degeneration, Source follower.	9
Module – 3	**No. of Hours**
Single stage Amplifier: common-gate stage, Cascade Stage, choice of device models.	9
Module – 4	**No. of Hours**
Differential Amplifiers: Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell.	9
Module – 5	**No. of Hours**
Passive and Active Current mirrors: Basic current mirrors, cascode current Mirrors, Active current mirrors – large signal analysis, small signal analysis, common mode properties. **Case Study** – Single stage op-amps, Two-stage op-amps.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Analyze the MOSFET I/V characteristics, second order effects.
CO2	Design single stage MOS common source amplifiers with various loads.
CO3	Design single stage MOS common gate and cascade stage.
CO4	Analyze the operation of differential amplifiers, Gilbert cell.
CO5	Analyze the operation of active and passive current mirrors.

Text Books	
1.	"BehzadRazavi", Design of Analog CMOS Integrated Circuits, TMH 2007.

Reference Text Books	
1.	"Phillip E.Allen, Douglas R.Holberg" ,CMOS Analog Circuit Design Oxford University Press 2nd Edition. 2016
2.	"R.JacobBaker", CMOS Circuit Design, Layout, and Simulation, Wiley 2nd Edition.2019

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	1	1	2	3	-	-	-	-	-	1
CO2	3	1	1	2	3	-	-	-	-	-	1
CO3	3	1	1	2	3	-	-	-	-	-	1
CO4	3	1	1	2	3	-	-	-	-	-	1
CO5	3	1	1	2	3	-	-	-	-	-	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-V					
Industry 4.0 and IoT **Category: PEC - I**					
Course Code	:	**B24EC564**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To understand the fundamental concepts, architecture, components, and applications of IoT systems along with sensors and actuators.
2.	To understand and analyze various communication protocols and interfacing techniques used in IoT systems.
3.	To develop skills in interfacing IoT devices, controlling hardware components, and working with different sensors.
4.	To understand the integration of IoT systems with cloud platforms and data communication services.
5.	To understand the design challenges and considerations involved in developing reliable and efficient IoT systems.

Module – 1	**No. of Hours**
Understanding Iot Concept and Development Platform: IOT Definition, Importance of IoT, Applications of IOT, IoT architecture, Understanding working of Sensors, Actuators, Sensor calibration, Study of Different sensors and their characteristics	9
Module – 2	**No. of Hours**
Analyzing & Decoding of Communication Protocol used in Iot Development Platform: UART Communication Protocol, I2C Protocol device interfacing and decoding of signal, SPI Protocol device interfacing and decoding of signal, WIFI and Router interfacing, Ethernet Configuration, Bluetooth study and analysis of data flow, Zigbee Interfacing and study of signal flow	9
Module – 3	**No. of Hours**
Iot Physical Devices and Endpoints: IoT Physical Devices and Endpoints- Introduction to Arduino and Raspberry Pi- Installation, Interfaces (serial, SPI, I2C), Programming – Python program with Raspberry PI with focus on interfacing external gadgets, controlling output, reading input from pins. **Controlling Hardware:** Connecting LED, Buzzer, Switching High Power devices with transistors, Controlling AC Power devices with Relays, Controlling servo motor, speed control of DC Motor, unipolar and bipolar Stepper motors; **Sensors:** Light sensor, temperature sensor with thermistor, voltage sensor, ADC and DAC, Temperature and Humidity Sensor DHT11, Motion Detection Sensors, Wireless Bluetooth Sensors, Level Sensors, USB Sensors, Embedded Sensors, Distance Measurement with ultrasound sensor.	9
Module – 4	**No. of Hours**
Cloud Services used in Iot Development Platform: Configuration of the cloud platform, Sending data from the IOT nodes to the gateways using different communication options; Transferring data from gateway to the cloud; Exploring the web services like mail, Messaging (SMS) and Twitter etc.; Tracking of cloud data as per the requirement; Google Cloud service architect; AWS clod Services architect; Microsoft Azure cloud services Architect; OEN source Cloud Services; Initial State Iot Dashboard & Cloud Services.	9
Module – 5	**No. of Hours**
Challenges in Iot System Design: HARDWARE & SOFTWARE: Antenna design and placement, Chip-package system development, Power electronics, electromagnetic interference/compatibility (EMI/EMC), Electronics reliability; Battery simulation.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Understand the building blocks of IoT technology and explore the vast spectrum of IoT applications.
CO2	Use processors & peripherals to design & build IoT hardware.
CO3	Assess, select and customize technologies for IoT applications.
CO4	Connect numerous IOT applications with the physical world of humans and real life problem solving.
CO5	Design and implement IOT applications that manage big data.

Text Books	
1.	Internet of Things - A Hands-on Approach, ArshdeepBahga and Vijay Madisetti, Universities Press, 2015, ISBN: 9788173719547
2.	Getting Started with Raspberry Pi, Matt Richardson & Shawn Wallace, O'Reilly (SPD), 2014, ISBN: 9789350239759

Reference Text Books	
1.	Raspberry Pi Cookbook, Software and Hardware Problems and solutions, Simon Monk, O'Reilly (SPD), 2016, ISBN 7989352133895
2.	N. Ida, Sensors, Actuators and Their Interfaces, SciTech Publishers, 2014.
3.	Peter Waher, 'Learning Internet of Things', Packt Publishing, 2015 3. Editors OvidiuVermesan

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	2	2	1	2	-	-	-	-	-
CO2	3	2	2	2	1	2	-	-	-	-	-
CO3	3	2	2	2	2	2	-	-	-	-	-
CO4	3	2	3	2	3	2	-	-	-	-	-
CO5	3	3	3	3	3	3	-	-	-	-	-

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-V					
Embedded Systems Design Lab **Category: AEC-V**					
Course Code	:	**B24EC581**	CIE	:	50 Marks
Teaching Hours L:T :P:S	:	0 : 0 : 2: 0	SEE	:	50 Marks
Total Hours	:	30	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To understand the fundamentals of Assembly Language Programming and instruction execution in microprocessors/microcontrollers.
2.	To develop Assembly Language Programs for arithmetic, logical, array, and data manipulation operations.
3.	To analyze and implement sorting, searching, and counting techniques using low-level programming concepts.
4.	To interface peripheral devices such as stepper motors, DACs, switches, LEDs, relays, buzzers, and 7-segment displays with embedded systems.
5.	To design and test embedded applications involving waveform generation, memory operations, and hardware interfacing techniques.

Sl. No	**List of Experiments**
1	Write a program to find the sum of the first 10 integer numbers.
2	Write an Assembly Language Program (ALP) to i) Multiply two 16-bit numbers. ii) Add two 32-bit numbers.
3	Write a program to find the factorial of a number.
4	Write a program to add an array of 16 bit numbers and store the 32 bit result in internal RAM.
5	Write a program to find the square of a number (1 to 10) using a look-up table.
6	Write a program to find the largest or smallest number in an array of 32 numbers
7	Write a program to arrange a series of 32 bit numbers in ascending/descending order.
8	i. Write a program to count the number of ones and zeros in two consecutive memory locations ii. Write an ALP to Scan a series of 32-bit numbers to find how many are negative.
9	Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
10	Interface a DAC and generate Triangular and Square waveforms
11	Display the Hex digits 0 to F on a 7-segment LED interface, with a suitable delay in between.
12	Interface a simple Switch and display its status through Relay, Buzzer and LED

Reference Text Books	
1.	Raj Kamal, “Embedded Systems: Architecture and Programming”, Tata McGraw Hill, 2008.
2.	Tammy Noergaard, ”Embedded System Architecture, A comprehensive Guide for Engineers and Programmers”, Elsevier, 2006
3.	Lyla B Das,” Embedded Systems-An Integrated Approach”, Pearson2013

Course Outcomes: At the end of the course, the students will be able to	
CO1	Develop and execute Assembly Language Programs for arithmetic, logical, and data processing operations.
CO2	Implement array handling, sorting, searching, and counting operations using low-level programmin techniques.
CO3	Apply memory organization concepts for handling multi-byte data operations and result storage.
CO4	Interface and control peripheral devices such as stepper motors, DACs, LEDs, relays, buzzers,

	switches, and 7-segment displays.
CO5	Design and test embedded system applications involving hardware interfacing and waveform generation.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Laboratory	**Lab Conduction & Record**	**Evaluating each expt. for 10 marks**	**20**	**50**
	Laboratory Test -1	**50**	**15**	
	Laboratory Test -2	**50**	**15**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
4. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
5. Change of experiment is allowed only once and 15% of Marks allotted to the Conduction procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	3	3	1	3	-	-	-	-	3	1
CO2	3	3	3	1	3	-	-	-	-	2	1
CO3	3	3	3	1	3	-	-	-	-	2	1
CO4	3	3	3	1	3	-	-	-	-	2	1
CO5	3	3	3	1	3	-	-	-	-	2	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-V					
Digital Image Processing Lab **Category: AEC-V**					
Course Code	:	**B24EC582**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	0:0:2:0	SEE	:	50 Marks
Total Hours	:	30	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To develop problem-solving skills through hands-on experiments and real-world image processing applications.
2.	To understand the fundamentals of digital image representation, pixel relationships, and intensity transformations and Learn to implement basic and advanced image processing techniques using Python and standard libraries.
3.	To analyze images in spatial and frequency domains using mathematical and computational tools.
4.	To apply image enhancement techniques such as contrast stretching, histogram processing, smoothing, and sharpening.
5.	To implement image compression and restoration techniques for efficient storage and improved image quality.

Sl. No.	**Title of the program / list of the experiment** **{List of Programs to be implemented & executed using any programming languages like MATLAB/PYTHON/OCTAVE (but not limited to)}**
1.	Simulation and Display of an Image, Negative of an Image (Binary & Gray Scale).
2.	Implementation of Relationships between Pixels.
3.	Implementation of Transformations of an Image.
4.	Contrast stretching of a low contrast image, Histogram, and Histogram Equalization.
5.	Display of bit planes of an Image.
6.	Display of FFT (1-D & 2-D) of an image.
7.	Computation of Mean, Standard Deviation, Correlation coefficient of the given Image.
8.	Implementation of Image Smoothening Filters (Mean and Median filtering of an Image).
9.	Implementation of image sharpening filters and Edge Detection using Gradient Filters.
10.	Image Compression by DCT, DPCM, HUFFMAN coding.
11.	Implementation of image restoring techniques.
12.	Implementation of Image Intensity slicing technique for image enhancement.

Course Outcomes: At the end of the course, the students will be able to	
CO1	Simulate, display, and manipulate digital images using Python programming tools.
CO2	Implement image intensity transformations including image negatives, pixel relationships, and intensity slicing for image enhancement.
CO3	Analyze image characteristics by computing statistical measures such as mean, standard deviation, correlation coefficient, and bit-plane representation.
CO4	Apply image enhancement techniques including contrast stretching, histogram generation, histogram equalization, smoothing, and sharpening filters
CO5	Analyze images in the frequency domain by implementing and interpreting 1-D and 2-D FFTs, and image compression and restoration techniques such as DCT, DPCM, Huffman coding, and image restoring filters for improving image quality and reducing data size

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Laboratory	**Lab Conduction & Record**	**Evaluating each expt. for 10 marks**	**20**	**50**
	Laboratory Test -1	**50**	**15**	
	Laboratory Test -2	**50**	**15**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
4. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
5. Change of experiment is allowed only once and 15% of Marks allotted to the Conduction procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	–	–	3	-	-	-	-	-	-
CO2	3	3	2	–	3	–	–	–	–	–	–
CO3	3	3	–	2	3	–	–	–	–	–	–
CO4	3	3	2	2	3	–	–	–	–	–	–
CO5	3	3	2	2	3	–	–	–	–	–	2

Level3 –High, Level2–Moderate, Level1 -Low

Semester-V					
Measurement and Controls Lab **Category: AEC-V**					
Course Code	:	**B24EC583**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	0:0:2:0	SEE	:	50 Marks
Total Hours/Semester	:	30	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To analyze the different types measuring instruments.
2.	To measure RLC parameters voltage, current, power, power factor, energy and magnetic measurements.
3.	To Carry out laboratory experiments on instruments, DC and AC bridges.
4.	To Understand the fundamentals of measuring instruments.
5.	To apply the above conceptual things to real-world electrical and electronics problems applications.

Sl. No	**List of Experiments**
1.	Calibration and Testing of Single Phase Energy Meter.
2.	Calibration of Dynamometer Type Power Factor Meter.
3.	Crompton DC Potentiometer – Calibration of PMMC Ammeter & PMMC Voltmeter.
4.	Kelvin's Double Bridge.
5.	Dielectric Oil Testing Using H.T Testing Kit.
6.	Schering Bridge & Anderson Bridge.
7.	Measurement of 3- Phase Reactive Power With Single Phase Wattmeter.
8.	Linear Variable Displacement Transducer.
9.	Calibration of LPF Wattmeter - By Phantom Testing.
10.	Measurement of 3- Φ Power Using Single Wattmeter and 2 No's of CT's.
11.	C.T Testing Using Mutual Inductor - Measurement of % Ratio Error And Phase angle of Given C.T by Null Method.
12.	P.T.Testing by Comparision Method Measurement of % Ratio Error And Phase angle of given P.T. by Comparison..
13.	Resistance strain gauge – strain measurements and Calibration.
14.	Transformer Turns Ratio Measurement Using A.C. Bridge.
15.	Measurement of % Ratio Error And Phase Angle of Given C.T. by Comparison.

Course Outcomes: At the end of the course, the students will be able to	
CO1	Analyze the different types measuring instruments
CO2	Measure RLC parameters voltage, current, power, power factor, energy and magnetic measurements
CO3	Carry out laboratory experiments on instruments, DC and AC bridges.
CO4	Understand the fundamentals of measuring instruments
CO5	Apply the above conceptual things to real-world electrical and electronics problems applications.

Reference Text Books	
1.	Measurements and Control, by Kishore N. Kawale, 2017.
2.	Measurement and Control Basics, 3rd Edition by Thomas A. Hughes,2002.
3.	Measurement and Laboratory Systems : A Comprehensive Guide by Anuj Bhatnagar,2015.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Laboratory	**Lab Conduction & Record**	**Evaluating each expt. for 10 marks**	**20**	**50**
	Laboratory Test -1	**50**	**15**	
	Laboratory Test -2	**50**	**15**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
4. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
5. Change of experiment is allowed only once and 15% of Marks allotted to the Copnduction procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	1	2							1
CO2	3	2	3	3							1
CO3	2	2	2	2							1
CO4	2	2	2	2							1
CO5	3	1	1	1							1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-V					
Industry 4.0 and IoT lab **Category: AEC-V**					
Course Code	:	**B24EC584**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	0:0:2:0	SEE	:	50 Marks
Total Hours	:	30	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To understand the core concepts and technologies of Industry 4.0 and IIoT.
2.	To learn about smart sensors, communication protocols, and data analytics.
3.	To develop practical skills in implementing IIoT solutions.
4.	To explore the impact of Industry 4.0 on industrial operations.
5.	To understand cyber security measures implemented in an IIoT system.

Sl. No.	**Title of the program / list of the experiment**
1.	a) Introduction to Software b) Pulsing LED
2.	Measurement of Temperature and Pressure using ESP32.
3.	Interfacing IR Sensor and OLED with ESP32.
4.	Interfacing Ultrasonic sensor with ESP32.
5.	Interfacing Soil Moisture sensor with ESP32.
6.	Interfacing Motor with ESP32.
7.	Interfacing Relay with ESP32.
8.	Interfacing Buzzer with ESP32.
9.	Demonstration of MQTT Communication.
10.	Visualization of Diverse Sensors data using Dashboard.
11.	Device Control using mobile Apps or through Web pages.
12.	Logic Gate Simulation.

Reference Books:	
1.	Internet of Things - A Hands-on Approach, Arshdeep Bahga and Vijay Madisetti, Universities Press, 2015, ISBN: 9788173719547
2.	Getting Started with Raspberry Pi, Matt Richardson & Shawn Wallace, O'Reilly (SPD), 2014, ISBN: 9789350239759

Course Outcomes: At the end of the course, the students will be able to	
CO1	Understand the core concepts and technologies of Industry 4.0 and Industrial IoT, including smart manufacturing, IoT devices, and communication protocols.
CO2	Explain the IoT communication protocols and integrate various IoT devices into a functional system for data collection and remote monitoring.
CO3	Analyze data from IIoT systems to derive actionable insights and evaluate the performance of predictive maintenance models in real-world scenarios.
CO4	Evaluate the cyber security measures implemented in an IIoT system and reflect on their effectiveness in safeguarding against potential threats and vulnerabilities
CO5	Design and develop an end-to-end IIoT solution, including system architecture, data processing, and integration with cloud platforms, to address a specific industrial application.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Laboratory	**Lab Conduction & Record**	**Evaluating each expt. for 10 marks**	**20**	**50**
	Laboratory Test -1	**50**	**15**	
	Laboratory Test -2	**50**	**15**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
4. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
5. Change of experiment is allowed only once and 15% of Marks allotted to the Conduction procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	3	-	2	-	-	-	-	-	1
CO2	3	3	2	-	2	-	-	-	-	-	1
CO3	3	2	3	-	2	-	-	-	-	-	1
CO4	3	3	2	-	2	-	-	-	-	-	1
CO5	3	3	2	2	2	-	-	-	-	-	1

Level 3 – High, Level 2 – Moderate, Level 1 -Low

Semester -V					
Mini - Project **Category: SDC**					
Course Code	:	**B24ECP511**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	0:0:4:0	SEE	:	50 Marks
Total Hours	:	60	Total	:	100 Marks
Credits	:	2	SEE Duration	:	3 Hrs

Mini-Project Work Evaluation:

Mini Project is a hands on course that will provide a platform to students to enhance their practical knowledge and skills by the development of small applications etc. Based on the ability/abilities of the student/s and recommendations of the supervisor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.

CIE procedure for Mini-project: (i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two faculty members of the Department, one of them being the Guide. The CIE marks awarded for the Mini-project work shall be based on the evaluation of the **Project Reviews, Project report and Viva-Voce in the ratio of 60:20:20**. The marks awarded for the project report shall be the same for all the batches mates.
(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the project.

CIE Evaluation: The CIE marks awarded for the Mini-project, shall be based on the evaluation of the **Project Reviews, Project report and Viva-Voce in the ratio of 60:20:20**. The marks awarded for the project report shall be the same for all the batches mates.

SEE Evaluation: SEE for project work will be conducted by the two examiners appointed by the Principal / CoE. The SEE marks awarded for the project work shall be based on the evaluation of **Write-up, Presentation Skills, Project Demonstration and Viva-Voce** in the ratio of 20:60:20

Rubrics for Mini-Project

Sl. No	**Criteria**	**Scale of Assessment**		
		Satisfactory (0-5)	**Good (6-8)**	**Excellent (9-10)**
1	Objective, Existing method with proposed method	Incomplete justification to the objectives proposed; Steps are mentioned but unclear; without justification to objectives	Good justification to the objectives; Methodology to be followed is specified but detailing is not done	All objectives of the proposed work are well defined. Steps to be followed to solve the defined problem are clearly specified.
2	Analysis/Description of the project	Incomplete explanation of the key concepts and in-sufficient description of the technical requirements of the project	Complete explanation of the key concepts but in-sufficient description of the technical requirements of the project	Complete explanation of the key concepts and strong description of the technical requirements of the project

3	Result Analysis	• All defined objectives are achieved. • Modules are working well in isolation and properly demonstrated • Modules of project are not properly integrated.	• All defined objectives are achieved. • Each module working well and properly demonstrated. • Integration of all modules not done and system working is not very satisfactory.	• All defined objectives are achieved. • Each module working well and properly demonstrated • All modules of project are well integrated and system working is accurate
4	Project Report	• Project report is according to the specified format but some mistakes. • In-sufficient references	• 1. Project report is according to the specified format. • References are appropriate but not mentioned well.	• Project report is according to the specified Format. • References are appropriate and well mentioned
5	Queries	Lacks sufficient knowledge and awareness	Fair knowledge and awareness related to the project.	Extensive knowledge and awareness related to the project

Semester-VI					
VLSI Design **Category: PCC**					
Course Code	:	**B24EC601**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	2:2:0:3	SEE	:	50 Marks
Total Hours	:	55	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To analyze digital CMOS integrated circuits.
2.	To emphasize on basic theory of digital circuits, design principles and techniques for digital design blocks implemented in CMOS technology.
3.	To analyze the switching characteristics of digital circuits along with delay and power estimation.
4.	To analyze the CMOS sequential circuits and memory design concepts.
5.	To explore the knowledge of VLSI Design flow and Testing.

Module – 1	**No.of Hrs**
Introduction to CMOS Circuits: Introduction, MOS Transistors, MOS Transistor switches, CMOS Logic, Alternate Circuit representation, CMOS-nMOS comparison.	11
Module – 2	**No.of Hrs**
MOS Transistor Theory: n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage, Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS inverter DC characteristics, Influence of βn / βp ratio on transfer characteristics, Noise margin, Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS.	11
Module – 3	**No.of Hrs**
CMOS Process Technology and Circuit characterization: CMOS Process Technology: Silicon Semiconductor Technology, CMOS Technologies, Layout Design Rules. [Text 1: 3.1,3.2,3.3.] Circuit Characterization and Performance Estimation: Introduction, Resistance Estimation, Capacitance Estimation, Switching Characteristics, CMOS gate transistor sizing, Determination of conductor size, Power consumption, Charge sharing, Scaling of MOS transistor sizing, Yield.	11
Module – 4	**No.of Hrs**
CMOS Circuit and Logic Design: Introduction, CMOS Logic structures, CMOS Complementary logic, Pseudo n-MOS logic, Dynamic CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch logic, Pass transistor Logic, Electrical and Physical design of Logic gates, The inverter, NAND and NOR gates, Body effect, Physical Layout of Logic gates, Input output Pads.	11
Module – 5	**No.of Hrs**
CMOS Subsytem design and Sequential MOS Logic Circuits: Combinational Adder, Transmission gate adder, Carry look ahead adder, Manchester carry adder, Binary counters – Asynchronous counter and Synchronous counters. Introduction, Behaviour of Bistable Elements (Excluding Mathematical analysis) SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, Clocked SR Latch, Clocked JK Latch.	11

Course Outcomes: At the end of the course, the students will be able to	
CO1	Apply the fundamentals of semiconductor physics in MOS transistors and analyze the geometrical effects of MOS transistors.
CO2	Design and realize combinational, sequential digital circuits and memory cells in CMOS logic.
CO3	Analyze the synchronous timing metrics for sequential designs and structured design basics.
CO4	Apply the concepts to design digital blocks with design constraints such as propagation delay and dynamic power dissipation.
CO5	Analyze the Sequential circuits and VLSI testing.

Text Books	
1.	Principals of CMOS VLSI Design A System approach Neil H E Weste and Kamran Eshraghain . Addition Wisley Publishing company,1988.
2.	"CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, 3rd Edition, Tata McGraw-Hill,2003.

Reference Text Books	
1.	"CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education.2010
2.	"Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

Web links and Video lectures (e-Resources)
1.https://youtu.be/faiEVOOCe-s?si=nfV7hqvTR6WfRcFw MOS transistor basics.
2. https://youtu.be/_gpEBYUnj6k?si=V5uAYVoN4DKZj0q8 MOSFET fabrication.
3. https://youtu.be/T2ztsyWpP5g?si=PuA-kTxSWBU6PLEr Logic and Fault simulation.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part –A and Part – B
3. **Part - A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 mark each. **Part - A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	-	1	1	-	-	-	-	-	-	1
CO2	3	-	1	1	-	-	-	-	-	-	1
CO3	3	-	1	1	-	-	-	-	-	-	1
CO4	3	-	1	1	-	-	-	-	-	-	1
CO5	3	-	1	1	-	-	-	-	-	-	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-VI					
Data Communication Networks **Category: IPCC**					
Course Code	:	**B24EC602**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:2:3	SEE	:	50 Marks
Total Hours	:	45+30	Total	:	100 Marks
Credits	:	4	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To explain the structure and functioning of layered network architectures.
2.	To identify networking components and describe their roles in communication systems.
3.	To design enterprise networks using LAN technologies and apply subnetting and routing concepts.
4.	To analyze the operation and features of application layer protocols such as HTTP, DNS, and SMTP.
5.	To identify and evaluate factors that enhance data communication network performance.

Module – 1	**No. of Hours**
Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet. **Network Models**: TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP. **Physical Layer:** Guided Media, Unguided Media (wireless). **Data-Link Layer:** Introduction: Nodes and Links, Services, Two Categories of link, Sublayers, Link Layer addressing: Types of addresses, ARP	9
Module – 2	**No. of Hours**
Data Link Control (DLC) services: Framing, Flow and Error Control. Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. **Connecting Devices:** Hubs, Switches, Virtual LANs: Membership, Configuration, Communication between Switches, Advantages. **Wired and Wireless LANs**: Ethernet Protocol, Standard Ethernet. **Introduction to wireless LAN**: Architectural Comparison, Characteristics, Access Control, Fast Ethernet, Gigabit Ethernet& IEEE802.11 wireless LANs	9
Module – 3	**No. of Hours**
Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution **Network Layer Protocols:** Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams), IPv6 addressing and Protocol **Unicast Routing:** Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path Vector Routing.), RIP, OSPF	9
Module – 4	**No. of Hours**
Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection-oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat protocol, Piggybacking **Transport-Layer Protocols in the Internet:** User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control L1, L2, L3 Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Error control, TCP congestion control.	9
Module – 5	**No. of Hours**
Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client – Server Protocols: Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS. Quality of Service , Network Security	9

Performance factors – Throughput, Bandwidth and Latency, High speed networks, Application performance needs.	

Course Outcomes: At the end of the course, the students will be able to	
CO1	Understand the details and functionality of layered network architecture.
CO2	Identify different networking components and their respective roles in a communication system.
CO3	Design an enterprise network employing the common LAN technologies and calculate and apply subnet masks and addresses and identify routing mechanisms to fulfil networking requirements.
CO4	Analyze the features and operations of various application layer protocols such as HTTP, DNS and SMTP.
CO5	Identify the key factors to improve the performance of data communication networks

LABORATORY

Practical Component of IPCC (12 Experiments)
Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/ QualNet or any other equivalent tool

Sl. No	Name of the experiments
1.	Implement a point-to-point network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
2.	Implement a four-node point-to-point network with links n0-n2, n1-n2, and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents, changing the parameter, and determine the number of packets sent by TCP/UDP.
3.	Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate. 5
4.	Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion window for different sources/ destinations.
5.	Implement ESS with transmission nodes in a Wireless LAN and obtain the performance parameters.
6.	Implementation of the link-state routing algorithm
	Implement the following using programming languages C/C++ etc,.
7.	Write a program for an HLDC frame to perform the following. i) Bit stuffing ii) Character stuffing.
8.	Write a program for the distance vector algorithm to find suitable path for transmission
9.	Implement Dijkstra‘s algorithm to compute the shortest routing path.
10.	For the given data, use CRC-CCITT polynomial to obtain the CRC code. Verify the program for the cases : i) without error ii)with error
11.	Implementation of the Stop and Wait Protocol and Sliding Window Protocol
12.	Write a program for congestion control using the leaky bucket algorithm

Text Books	
1.	Forouzan, “Data Communications and Networking”, 5th Edition, McGraw Hill, 2013, ISBN: 1-25- 906475-3
2.	Larry L.Peterson and Bruce S.Davie, “Computer Networks: A Systems Approach”, Morgan Kaufmann Publishers., San Francisco, 4th Edition, 2007.

Reference Text Books	
1.	J.F. Kurose & K.W. Ross,” Computer Networking- A top down approach featuring the internet”, Pearson, 2nd edition, 2012.
2.	Andrew S. Tanenbaum, “Computer Networks”, PHI, Fourth Edition, 2011.
3.	Dimitri Bertsekas and Robert Gallager, “Data Networks” Prentice hall of India Pvt. Ltd., 2nd edition, 1994.

4	Bhusan Trivedi - Data communication and Networks, Oxford university press, 2016
Web links and Video lectures (e-Resources):	
1.http://www.digimat.in/nptel/courses/video/117105148/L02.html 2.https://www.youtube.com/playlist?list=PLEAYkSg4uSQ2NMmzNNsEK5RVbhxqx0BZF 3.http://www.digimat.in/nptel/courses/video/106105183/L54.html	

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**30** (Average of Best Two Assessments)	**50/2 = 25**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	Any One Assessments as per regulations	**20**	**20**	
Laboratory	**Lab conduction & Record**	Evaluating each expt. for 10 marks.	**05**	**25**
	Internal Test	**50**	**20**	
Total Marks				**50**
SEE	**Semester End Examination**	**100**	**50**	**50**
Total marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice. Students should answer five full questions, selecting one full question from each module.
5. Students have to answer for 100 marks and marks scored out of 100 shall be proportionally reduced to 50 marks.
6. The maximum marks from the practical component to be included in the SEE question paper is **16 marks.**
7. Question papers to be set as per the Blooms Taxonomy levels.
8. The laboratory component of the **integrated course** shall be CIE only. However, in SEE, the questions from the practical component shall be included.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	1	-	-	1	-	-	2	2	2	-
CO2	2	1	-	-	2	-	-	2	2	2	1
CO3	3	2	1	-	2	-	-	2	2	1	2
CO4	3	3	2	-	2	-	-	2	3	1	1
CO5	3	2	1	-	2	-	-	2	3	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester -VI					
Multimedia Communication **Category: PEC-II**					
Course Code	:	**B24EC631**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To gain fundamental knowledge in understanding the basics of different multimedia Networks and applications.
2.	To understand digitization principle techniques required to analyze different media Types.
3.	To analyze compression techniques required to compress text and image and gain Knowledge of DMS.
4.	To analyze compression techniques required to compress audio and video.
5.	To gain fundamental knowledge about multimedia communication across different Networks.

Module – 1	**No.of Hrs**
Multimedia Communications: Introduction, Multimedia information representation, Multimedia networks, multimedia applications, Application and networking terminology.	9
Module – 2	**No.of Hrs**
Information Representation: Introduction, Digitization principles, Text, Images, Audio and Video.	9
Module – 3	**No.of Hrs**
Text and Image Compression: Introduction, Compression principles, text compression, image Compression.	9
Module – 4	**No.of Hrs**
Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression. Multimedia Information Networks: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI	9
Module – 5	**No.of Hrs**
Multimedia information representation : Multimedia networks, multimedia applications, Application and networking terminology, network QoS and application QoS, Digitization principles,. Text, images, audio and video.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Express the basics of multimedia Communication and applications.
CO2	Analyze media types to represent them in digital form.
CO3	Understand about Text and Image Compression.
CO4	Apply the compression techniques on text, images, audio and video.
CO5	Understand multimedia information networks.

Text Books	
1.	Multimedia Communications –Fred Halsall, Pearson Education, 2001,ISBN-978813170994.
2.	K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, “Multimedia Communication Systems”, Pearson education, 2004.

Reference Text Books	
1.	Multimedia: Computing, Communications and Applications- Raif Steinmetz, Klara Nahrstedt, Pearson Education, 2002, ISBN-978817758
2.	John Billamil, Louis Molina, “Multimedia : An Introduction”, PHI, 2002.

Web links and Video lectures (e-Resources)
1. Implementation of compression algorithms using MATLAB/any open source tools (Python, Scilab, etc.) 2 https://www.slideshare.net/ NPTEL Video Lectures 3. https://archive.nptel.ac.in/courses/117/105/117105083/ 4. Multimedia Computing lecture: Communications & Networking –You Tube

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	Internal Assessment-1	50	30 (Average of Best two Assessments)	50
	Internal Assessment-2	50		
	Internal Assessment-3	50		
AAT	Two Assessments as per regulations	20	20	
SEE	Semester End Examination	100	50	50
Total Marks				100

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part –A and Part – B
3. **Part - A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 mark each. **Part - A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	1	-	-	-	3	1	-	-	1	-
CO2	2	2	-	-	-	2	1	-	-	2	-
CO3	1	1	-	-	-	1	2	-	-	2	-
CO4	1	1	-	-	-	1	2	-	-	1	-
CO5	1	1	-	-	-	1	2	-	-	1	-

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-VI					
Neural Networks **Category: PEC-II**					
Course Code	:	**B24EC632**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To provide exposure to the basic concepts, models, and learning mechanisms of Artificial Neural Networks.
2.	To enable students to solve simple problems using feedforward and feedback neural network architectures.
3.	To impart knowledge of associative memory models, global minima networks, and competitive neural networks.
4.	To develop an understanding of Adaptive Resonance Theory (ART) and its neural network models.
5.	To enable students to apply neural network techniques in pattern and speech recognition applications.

Module– 1	**No. of Hrs**
Introduction: Artificial neural networks - History-Structure and function of single neuron-Weights, activation functions and bias Fundamental neuron models and learning-Neural net architectures-Learning algorithms, supervised and unsupervised -Use of neural networks - Perceptron- linear separability.	9
Module– 2	**No. of Hrs**
Feed Forward and Feedback Networks: Back propagation network-Architecture -Delta rule-Weight updation for output and hidden layer - Local and global minima-practical considerations–Merits, demerits and applications-Pattern association-Associative memories-BAM-Energy theorem-Architecture and processing-Hopfield memory-Discrete and continuous -Optimization using hopfield networks	9
Module– 3	**No. of Hrs**
Simulated Annealing and Competitive Networks: Annealing-Boltzman machine architecture, learning and processing-Practical considerations-Neural networks based on competition-Counter propagation network-Forward mapping CPN and complete CPN-Building blocks-Architecture, Training and data processing-Practical considerations and applications	9
Module– 4	**No. of Hrs**
Som and Adaptive Resonance Theory: Topologically organized network-Feature map classifier-Applications-Learning vector quantizationAdaptive resonance theory-Fundamentals-Basic architecture and operation-Pattern matching-ART1 network - Architecture and processing summary	9
Module– 5	**No. of Hrs**
Handwritten Character and Speech Recognition: Neocognitron-Architecture-Data processing and performance-Spatio-temporal pattern classificationSTN- Architecture-Speech recognition-SCAF-Training -Time dilation effect	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Apply the basic concepts, architectures, and learning mechanisms of Artificial Neural Networks.
CO2	Analyze and solve simple problems using feedforward and feedback neural network models.
CO3	Apply and compare associative memory models, global minima networks, and competitive neural networks.
CO4	Analyze of Adaptive Resonance Theory (ART) and its neural network architectures.
CO5	Apply neural network techniques to pattern recognition and speech recognition applications.

Text Books	
1.	James A. Freeman, David M. Skapura, "Neural Networks Algorithms, Applications, and Programming Techniques", Pearson Education (Singapore) Private Limited, Delhi, 2011
2.	Satish Kumar, "Neural Networks: A Classroom Approach", Second Edition Tata McGraw-Hill Publishing Company Limited, New Delhi, 2013
Reference Text Books	
1.	Simon Haykin, "Neural Networks: A Comprehensive Foundation", 2nd edition,Prentice-Hall of India, 2008.
2.	Laurence Fausett, "Fundamentals of neural networks, Architectures, Algorithms and Applications", Pearson education Private Limited, Delhi, 2004.

3.	Sivanandam.S.N, Sumathi.S, Deepa.S.N, "Introduction to Neural networks using MATLAB 6.0", Tata McGraw-Hill Publishing Company Limited, New Delhi, 2010, 10th reprint.

Web links and Video lectures (e-Resources)
1.NPTEL – Artificial Neural Networks https://nptel.ac.in/courses/106/106/106106184/
2MIT OpenCourseWare – Neural Networkshttps://ocw.mit.edu
3.Simplilearn – Neural Networks Tutorialhttps://www.youtube.com/ @ Simplilearn Official
4. **Artificial Neural Network Tutorial – Edureka (YouTube)** – Beginner-friendly video on basics like perceptrons and multilayer networks. Watch ANN Tutorial on YouTube (Edureka)

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part –A and Part – B
3. **Part - A** should contain minimum **Two or Four**quiz questions from each module of 02 marks/ 01 mark each. **Part - A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	2	-	-	-	-	-	-	-	-
CO2	3	2	2	-	-	-	-	-	-	-	-
CO3	3	2	2	-	-	-	-	-	-	-	-
CO4	3	2	2	-	-	-	-	-	-	-	-
CO5	3	2	2	-	-	-	-	-	-	-	-

Level 3- High, Level 2- Moderate, Level 1-Low

Semester-VI					
RTOS(Real Time Operating Systems) **Category: PEC-II**					
Course Code	:	**B24EC633**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits		3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To acquire knowledge about concepts related o real time systems.
2.	To acquire knowledge about different types of scheduling algorithms.
3.	To study about Free RTOS.
4.	To understand the various functions of RTOS.
5.	To develop RTOS based applications.

Module – 1	**No.of Hrs**
Real time systems and Resources: Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems, Requirements of Embedded System, Challenges in Embedded System. System Resources, Resource Analysis, Real-Time Service Utility. Processing with Real Time Scheduling: Scheduler Classes, Preemptive Fixed Priority, Scheduling Policies with timing diagrams, Rate Monotonic least upper bound, Necessary and Sufficient feasibility ,Deadline–Monotonic Policy, Dynamic priority policies, Worst case execution time, Deadlock and live lock.	9
Module – 2	**No.of Hrs**
Real Time Operating Systems: Operating System basics, The Kernelan ditssub systems, Kernel Space and User Space, Kernel Architecture, Types of operating system, Task, process and Threads, Multi- Processing and Multi tasking, Types of multitasking, Task Scheduling, Task states, Non-Preemptive scheduling, Preemptive Scheduling, Round Robin Scheduling, Idle Task, Task Communication, Task Synchronization, Thread Safe Reentrant Functions.	9
Module – 3	**No.of Hrs**
Embedded Firmware Design ,development and Free RTOS: Embedded Firmware Design Approaches, Super-loop based approach, Embedded Operating System based approach, Programming in Embedded C, Integrated development environment(IDE), Overview of IDEs for Embedded System Development. Introduction to Free RTOS, multitasking on an LPC17xx Cortex-M3 Microcontroller, LPC17xx Port of Free RTOS, Resources Used by Free RTOS, Task Management, Task Functions, Task Priorities ,Idle task and task hook function, Creation and Deletion of tasks.	9
Module – 4	**No.of Hrs**
Embedded System design with Free RTOS: Queue Management, Characteristics of a Queue, Working with Large Data, Interrupt Management, Queues within an Interrupt Service Routine, Critical Sections and Suspending the Scheduler, Resource Management, Memory Management.	9
Module – 5	**No.of Hrs**
Design Examples and Case Studies of Progam Modeling and Programming With RTOS: Case study of Communication between Orchestra Robots, Embedded Systems in Automobile, Case study of an Embedded System for an Adaptive Cruise Control(ACC) System in a Car, Case study of an Embedded System for a Smart Card, Case study of a Mobile Phone Software for Key Inputs.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Express the fundamental concepts of RTOS.
CO2	Classify and exemplify scheduling algorithms.
CO3	Design and develop the embedded firm ware.
CO4	Analize the basic concepts of Free RTOS.
CO5	Design an embedded system with Free TOS and Use commercial tools to develop RTOS based applications.

Text Books	
1.	Sam Siewert, “Real-Time Embedded Systems And Components”,2007.
2.	Introduction to Embedded System- Shibu KV, Mc-Graw Hill Higher Edition,2009.

Reference Text Books	
1.	"Using the Free RTOS Real Time Kernel "From Free RTOS,2011.
2.	Embedded Systems Architecture, Programming and Design- Raj Kamal, 2nd Edition, McGraw-Hill Companies,2008.

Web links and Video lectures (e-Resources)
1. https://intellipaat.com/blog/real-time-operating-system/
2 https://youtu.be/tDX5T8NREts?si=Jo8wcQHWbrl2sW3y
3. https://youtu.be/TxPoj1skMHA?si=OQmISfG6PlbRn3R5

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part –A and Part – B
3. **Part - A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 mark each. **Part - A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	1	-	-	-	3	1	-	-	1	2
CO2	2	2	-	-	-	2	1	-	-	2	2
CO3	1	1	-	-	-	1	2	-	-	2	1
CO4	1	1	-	-	-	1	2	-	-	1	1
CO5	1	1	-	-	-	1	2	-	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-VI					
Digital Circuit Design using Verilog **Category: PEC-II**					
Course Code	:	**B24EC634**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits		3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To understand the types of programmable logic devices, ASIC classifications, and the fundamental building blocks of FPGAs.
2.	To understand advanced logic design concepts and implement digital circuits using Verilog HDL and programmable ASIC logic cells.
3.	To design and implement different digital applications using SM charts and microprogramming techniques.
4.	To understand floating-point arithmetic representation, multi-valued logic concepts, and signal resolution techniques in digital system design.
5.	To implement and analyze digital system designs using Xilinx FPGAs, including routing, placement, and performance evaluation.

Module – 1	**No.of Hrs**
Introduction to Programmable Logic Devices: Brief overview of Programmable Logic Devices, Simple Programmable Logic Devices (SPLDs), Complex Programmable Logic devices (CPLDs), Field-Programmable Gate Arrays (FPGAs)	9
Module – 2	**No.of Hrs**
Advanced Digital Design Examples: BCD to 7-Segment Display Decoder, BCD Adder, Traffic Light Controller, Synchronization and debouncing, Shift-and-Add Multiplier, Array Multiplier, Keypad Scanner (Excluding Test Bench)	9
Module – 3	**No.of Hrs**
SM Charts and Microprogramming: State Machine Charts, Derivation of SM Charts, SM chart for binary multiplier, Dice Game (Excluding Test Bench), Realization of SM Charts, Implementation of the Dice Game. Microprogramming, Linked State Machines.	9
Module – 4	**No.of Hrs**
Floating-Point Arithmetic & Multi valued Logic and Signal Resolution: Representation of Floating-Point Numbers, Floating-Point Addition, Other Floating-Point Operations. Built-in Primitives, User-Defined Primitives, SRAM Model, Rise and Fall Delays of Gates, Model for SRAM Read/Write System, Rise and Fall Delays of Gates.	9
Module – 5	**No.of Hrs**
Designing with Field Programmable Gate Arrays: Implementing Functions in FPGAs, Implementing Functions Using Shannon's Decomposition, Carry Chains in FPGAs, Cascade Chains in FPGAs, Examples of Logic Blocks in Commercial FPGAs, Dedicated Multipliers in FPGAs, FPGAs Capacity: Maximum gates versus Usable gates, Design Translation.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Apply the concept of Programmable logic devices to implement digital design.
CO2	Design and implementation of Advanced logic design using Verilog HDL.
CO3	Apply the concept of SM Chart and design complex digital circuits using SM Chart.
CO4	Express the Floating-point arithmetic operations and designing of Memories.
CO5	Evaluate the Performance of advanced digital design using FPGAs.

Text Books	
1.	Digital Systems Design Using Verilog First Edition, 2014, Charles H. Roth, Jr. The University of Texas at Austin, Lizy Kurian John The University of Texas at Austin, ByeongKil Lee The University of Texas at San Antonio.

Reference Text Books	
1.	Advanced FPGA Design Architecture, Implementation, and Optimization, Steve, Spectrum Design Solutions Minneapolis, Minnesota, 2007
2.	ASIC and FPGA Verification: A guide to component Modelling. Richard Munden, Morgan Kaufmann Publishers is an imprint of Elsevier 2005
3.	Processor Design, System-on-Chip Computing for ASICs and FPGAs, JariNurmi Finland Tampere University of Technology Sringer Publications.2007
4.	The design Warrior's guide to FPGA Clive 'Max' Maxfield Elsevier Publications, 2004

Web links and Video lectures (e-Resources)
1.https://youtu.be/EQMWuZ_3_Is?si=bsfQBDkluJviGRMc
2.https://youtu.be/msXKWn24TN4?si=EvcEa7CmBai9zrrJ
3.https://youtu.be/JCxE3JQAXY0?si=6QD50NgWD-wk9_bU

ASSESSMENT DETAILS BOTH (CIE AND SEE)

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CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part –A and Part – B
3. **Part - A** should contain minimum **Two or Four**quiz questions from each module of 02 marks/ 01 mark each. **Part - A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
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CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	1	1	2	-	2	-	-	-	-	-	1
CO2	2	3	2	-	3	-	-	-	-	-	1
CO3	1	1	2	-	2	-	-	-	-	-	1
CO4	1	1	2	-	2	-	-	-	-	-	1
CO5	3	3	2	-	3	-	-	-	-	-	1

Level 3- High, Level 2- Moderate, Level 1-Low

Semester -VI					
Digital Electronics for Engineers **Category: OEC-I**					
Course Code	:	**B24EC641**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 hrs

Course Learning Objective is	
1.	To provide basic understanding of properties and theorems of Boolean Algebra.
2.	To provide knowledge on logic gates and universal gates.
3.	To teach techniques to reduce the Boolean expressions using K map.
4.	To give introduction to Logic families and different types Integrated circuits.
5.	To provide concept of Integrated Circuits.

Module – 1	**No. of Hours**
Number Systems: Number systems, Complements of Numbers, Codes- Weighted and Non weighted codes and its Properties. Boolean Algebra: Basic Theorems and Properties, Switching Functions- Canonical and Standard Form, Algebraic Simplification, Digital Logic Gates, EX-OR gates, Universal Gates, Multilevel NAND/NOR realizations.	9
Module – 2	**No. of Hours**
Minimization of Boolean functions: Karnaugh Map Method - Up to four Variables, Don't Care Map Entries, Tabular Method, Combinational Logic Circuits: Adders, Subtractors, Comparators, Multiplexers, Demultiplexers, Encoders, Decoders and Code converters, Hazards and Hazard Free Relations.	9
Module – 3	**No. of Hours**
Sequential Circuits Fundamentals: Basic Architectural Distinctions between Combinational and Sequential circuits, SR Latch, Flip Flops: SR, JK, JK Master Slave, D and T Type Flip Flops, Excitation Table of all Flip Flops, Fundamentals of shift registers, ripple and decade counter.	9
Module – 4	**No. of Hours**
Realization of Logic Gates Using Diodes & Transistors: AND, OR and NOT Gates using Diodes and Transistors, DCTL, RTL, DTL, TTL, CML and CMOS Logic Families and its Comparison, standard TTL NAND Gate Analysis & characteristics, TTL open collector O/Ps, Tristate TTL, MOS & CMOS open drain and tristate outputs, CMOS transmission gate,	9
Module – 5	**No. of Hours**
Integrated Circuits: Classification, chip size and circuit complexity, basic information of Op amp, ideal and practical Op-amp, internal circuits, Op-amp characteristics, DC and AC Characteristics, 741 opamp and its features, modes of operation-inverting, non-inverting, differential.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Get basic knowledge on logic gates, Universal gates and their switching logics.
CO2	Realize Boolean expressions using NAND/NOR gates and reduce them using K map.
CO3	Know all types of combinational and sequential circuits.
CO4	Acquire knowledge on realization of logic families using diodes and transistor
CO5	Acquire knowledge on different types of integrated circuits.

Text Books	
1.	Switching and Finite Automata Theory - ZviKohavi&Niraj K. Jha, 3rd Edition, Cambridge, 2010.
2.	Modern Digital Electronics – R. P. Jain, 3rd Edition, 2007- Tata McGraw-Hill
3.	Linear Integrated Circuits, D. Roy Chowdhury, 2004,New Age International(p) Ltd.
4.	Op-Amps & Linear ICs, Ramakanth A. Gayakwad, 2000, PHI

Reference Text Books	
1.	Digital Design- Morris Mano, 6th edition 2018, PHI,
2.	Operational Amplifiers & Linear Integrated Circuits, R.F. Coughlin & Fredrick F. Driscoll, 1990, PHI
3.	Operational Amplifiers & Linear Integrated Circuits: Theory & Applications, Denton J. Daibey, 1989, TMH.

Web links and Video lectures (e-Resources)
https://nptel.ac.in/courses/108105132

ASSESSMENT DETAILS BOTH (CIE AND SEE)

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CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	1	1	2	-	1	-	-	-	1	-	1
CO2	2	2	3	2	1	-	-	-	1	-	1
CO3	1	1	2	1	1	-	-	-	1	-	1
CO4	1	1	1	-	1				1		1
CO5	1	1	1	1	1				1		1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-VI					
Basics of VLSI **Category: OEC -I**					
Course Code	:	**B24EC642**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Learninmg Objective is	
1.	To analyze digital CMOS integrated circuits.
2.	To emphasize on basic theory of digital circuits, design principles and techniques for digital design blocks implemented in CMOS technology.
3.	To analyze the switching characteristics of digital circuits along with delay and power estimation.
4.	To analyze the CMOS sequential circuits and memory design concepts.
5.	To explore the knowledge of VLSI Design flow and Testing.

Module – 1	**No.of Hrs**
Introduction to CMOS Circuits: Introduction, MOS Transistors, MOS Transistor switches, CMOS Logic, Alternate Circuit representation, CMOS-nMOS comparison.	9
Module – 2	**No.of Hrs**
MOS Transistor Theory: n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage, Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS inverter DC characteristics, Influence of βn / βp ratio on transfer characteristics, Noise margin, Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS.	9
Module – 3	**No.of Hrs**
CMOS Process Technology and Circuit characterization: CMOS Process Technology: Silicon Semiconductor Technology, CMOS Technologies, Layout Design Rules. Circuit Characterization and Performance Estimation: Introduction, Resistance Estimation, Capacitance Estimation, Switching Characteristics, CMOS gate transistor sizing, Determination of conductor size, Power consumption, Charge sharing, Scaling of MOS transistor sizing, Yield.	9
Module – 4	**No.of Hrs**
CMOS Circuit and Logic Design: Introduction, CMOS Logic structures, CMOS Complementary logic, Pseudo n-MOS logic, Dynamic CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch logic, Pass transistor Logic, Electrical and Physical design of Logic gates, The inverter, NAND and NOR gates, Body effect, Physical Layout of Logic gates, Input output Pads.	9
Module – 5	**No.of Hrs**
CMOS Subsytem design and Sequential MOS Logic Circuits: Combinational Adder, Transmission gate adder, Carry look ahead adder, Manchester carry adder, Binary counters – Asynchronous counter and Synchronous counters. Introduction, Behaviour of Bistable Elements (Excluding Mathematical analysis) SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, Clocked SR Latch, Clocked JK Latch.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Apply the fundamentals of semiconductor physics in MOS transistors and analyze the geometrical effects of MOS transistors
CO2	Design and realize combinational, sequential digital circuits and memory cells in CMOS logic.
CO3	Analyze the synchronous timing metrics for sequential designs and structured design basics.
CO4	Apply the concepts to design digital blocks with design constraints such as propagation delay and dynamic power dissipation.
CO5	Analyze the Sequential circuits and VLSI testing.

Text Books	
1.	Principals of CMOS VLSI Design A System approach Neil H E Weste and Kamran Eshraghain . Addition Wisley Publishing company,1988.
2.	"CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, 3rd Edition, Tata McGraw-Hill,2003.

Reference Text Books	
1.	"CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education.2010
2.	"Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

Web links and Video lectures (e-Resources)
1. https://youtu.be/faiEVOOCe-s?si=nfV7hqvTR6WfRcFw MOS transistor basics.
2. https://youtu.be/_gpEBYUnj6k?si=V5uAYVoN4DKZj0q8 MOSFET fabrication.
3. https://youtu.be/T2ztsyWpP5g?si=PuA-kTxSWBU6PLEr Logic and Fault simulation.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

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Theory	**Internal Assessment-1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
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3. **Part - A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 mark each. **Part - A is Compulsory** and carries 20 Marks.
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5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
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PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
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CO2	3	-	1	1	-	-	-	-	-	-	1
CO3	3	-	1	1	-	-	-	-	-	-	1
CO4	3	-	1	1	-	-	-	-	-	-	1
CO5	3	-	1	1	-	-	-	-	-	-	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-VI					
Communication Systems **Category: OEC-I**					
Course Code	:	**B24EC643**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits		3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To understand and analyse concepts of Analog Modulation schemes viz; AM, FM.
2.	To design and analyse the electronic circuits for AM and FM modulation and demodulation.
3.	To understand the concepts of random variable and random process to model communication systems.
4.	To understand and analyse the concepts of digitization of signals.
5.	To evolve the concept of SNR in the presence of channel induced noise.

Module– 1	**No.of Hrs**
Random Variables and Processes: Introduction, Probability, Conditional Probability, Random variables. Statistical Averages: Function of a random variable, Moments, Random Processes, Mean, Correlation and Covariance function: Properties of autocorrelation function, Cross–correlation functions, Gaussian Process: Gaussian Distribution Function.	9
Module– 2	**No.of Hrs**
Amplitude Modulation Fundamentals: AM Concepts, Modulation index and Percentage of Modulation, Sidebands and the frequency domain, AM Power, Single Sideband Modulation. AM Circuits: Amplitude Modulators: Diode Modulator, Transistor Modulator, collector Modulator. Amplitude Demodulators: Diode Detector, Balanced Modulators: Lattice Modulators. Frequency Division Multiplexing: Transmitter-Multiplexer, Receiver-Demultiplexer.	9
Module– 3	**No.of Hrs**
Fundamentals of Frequency Modulation: Basic Principles of Frequency Modulation, Principles of Phase Modulation, Modulation index and sidebands, Noise Suppression Effects of FM, Frequency Modulation versus Amplitude Modulation. FM Circuits: Frequency Modulators: Voltage Controlled Oscillators. , Frequency Demodulators: Slope Detectors, Phase Locked Loops. Communication Receiver: Super heterodyne receiver, Frequency Conversion: Mixing Principles, JFET Mixer.	9
Module– 4	**No.of Hrs**
Digital Representation of Analog Signals: Introduction, Digitize Analog Sources, The Sampling process, Pulse Amplitude Modulation, Time-Division Multiplexing, Pulse Position Modulation: Generation and Detection of PPM wave. The Quantization Process. Pulse Code Modulation: Sampling, Quantization, Encoding, line Codes, Differential encoding, Regeneration, Decoding, filtering, multiplexing.	9
Module– 5	**No.of Hrs**
Baseband Transmission of Digital signals: Introduction, Intersymbol Interference, Eye Pattern, Nyquist criterion for distortionless Transmission, Baseband M-ary PAM Transmission. Noise: Signal to Noise Ratio, External Noise, Internal Noise, Semiconductor Noise, Expressing Noise Levels, Noise in Cascade Stages.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Understand the principles of analog communication systems and noise modelling.
CO2	Identify the schemes for analog modulation and demodulation and compare their performance.
CO3	Design of PCM systems through the processes sampling, quantization and encoding.
CO4	Describe the ideal condition, practical considerations of the signal representation for baseband transmission of digital signals
CO5	Identify and associate the random variables and random process in Communication system design.

Text Books	
1.	Louis E Frenzel, Principles of Electronic Communication Systems, 3rd Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-0-07-066755-6.
2.	Simon Haykin& Michael Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN: 978-81-265-2151-7

Reference Text Books	
1.	B P Lathi, Zhi Ding, "Modern Digital and Analog Communication Systems", Oxford University Press., 4th edition, 2010, ISBN: 97801980738002.
2.	Herbert Taub, Donald L Schilling, GoutamSaha, "Principles of Communication systems", 4th Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-1-25-902985-1

Web links and Video lectures (e-Resources)
Principles of Communication Systems https://nptel.ac.in/courses/108104091
Communication Engineering https://nptel.ac.in/courses/117102059

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	**Type of Assessment**	**Max. Marks**	**Max. Marks Scaling Down to**	**Total Marks**
Theory	**Internal Assessment-1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	-	-	-	-	-	-	-	1	1
CO2	3	3	2	-	2	-	-	-	-	1	1
CO3	2	3	2	-	2	-	-	-	-	1	1
CO4	2	3	2	2	3	-	-	-	-	1	1
CO5	2	2	3	3	3	-	-	-	-	1	1

Level 3- High, Level 2- Moderate, Level 1-Low

Semester -VI					
Electronics in Agricultural system **Category: OEC-I**					
Course Code	:	**B24EC644**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	3:0:0:3	SEE	:	50 Marks
Total Hours	:	45	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To understand the concept of Precision Farming.
2.	To understand the concepts of Environment Control Systems.
3.	To understand the idea of Agricultural Systems Management.
4.	To understand the basic of Weather Prediction Models.
5.	To understand the different E-Governance In Agricultural Systems.

Module – 1	**No. of Hours**
Precision Farming: Precision agriculture and agricultural management – Ground based sensors, Remote sensing, GPS, GIS and mapping software, Yield mapping systems, Crop production modeling.	9
Module – 2	**No. of Hours**
Environment Control Systems: Artificial light systems, management of crop growth in greenhouses, simulation of CO2 consumption in greenhouses, on-line measurement of plant growth in the greenhouse, models of plant production and expert systems in horticulture.	9
Module – 3	**No. of Hours**
Unit Iii Agricultural Systems Management: Agricultural systems - managerial overview, Reliability of agricultural systems, Simulation of crop growth and field operations, Optimizing the use of resources, Linear programming, Project scheduling, Artificial intelligence and decision support systems.	9
Module – 4	**No. of Hours**
Weather Prediction Models: Importance of climate variability and seasonal forecasting, Understanding and predicting world's climate system, Global climatic models and their potential for seasonal climate forecasting, General systems approach to applying seasonal climate forecasts.	9
Module – 5	**No. of Hours**
E-Governance In Agricultural Systems: Expert systems, decision support systems, Agricultural and biological databases, e-commerce, e business systems & applications, Technology enhanced learning systems and solutions, e-learning, Rural development and information society..	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	The students shall be able to understand the applications of IT in remote sensing applications such as Drones etc.
CO2	The students will be able to get a clear understanding of how a greenhouse can be automated and its advantages
CO3	The students will be able to apply IT principles and concepts for management of field operations.
CO4	The students will get an understanding about weather models, their inputs and applications.
CO5	The students will get an understanding of how IT can be used for e-governance in agriculture.

Text Books	
1.	National Research Council, "Precision Agriculture in the 21st Century", National Academies Press, Canada, 1997.
2.	H. Krug, Liebig, H.P. "International Symposium on Models for Plant Growth, Environmental Control and Farm Management in Protected Cultivation", 1989.

Reference Text Books	
1.	Peart, R.M., and Shoup, W. D., "Agricultural Systems Management", Marcel Dekker, New York 2004.
2.	Hammer, G.L., Nicholls, N., and Mitchell, C., "Applications of Seasonal Climate", Springer, Germany, 2000.

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	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per regulations**	**20**	**20**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
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CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
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CO2	3	3	3	3	-	-	-	-	-	3	3
CO3	2	3	3	2	-	-	-	-	-	3	3
CO4	3	3	3	1	-	-	-	-	-	3	3
CO5	2	3	3	2	-	-	-	-	-	3	3

1 - low, 2 - medium, 3 - high, '-"- no correlation

Semester-VI					
VLSI Design Laboratory **Category: PCCL**					
Course Code	:	**B24EC605L**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	0:0:2:0	SEE	:	50 Marks
Total Hours	:	30	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To study the design, modelling, simulation and verification of sequential circuits using the behavioural, gate level and data flow modelling.
2.	To study the design, modelling, simulation and verification of combinational circuits using the behavioural, gate level and data flow modelling.
3.	To study the design, simulation and verification of various CMOS logic gates at transistor level.
4.	To study the layout design of various CMOS logic gates.
5.	To study the RTL-GDSII flow and understand the ASIC Design flow.

Sl. No	**List of Experiments**
1.	Design a 4-Bit Adder • Write a Verilog description • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and generate the gate level netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required.
2.	4-Bit Shift and add Multiplier • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the gate level netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required.
3.	32-Bit ALU Supporting 4-Logical and 4-Arithmetic operations, using case and if statement for ALU BehavioralModeling • Write Verilog description • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist • Identify Critical path
4.	Flip-Flops (D,SR and JK) • Write the Verilog description • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the gate level netlist. From the report gate level netlist identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required. • Verify the functionality using Gate level netlist and compare the results at RTL and gate level netlist.
5.	Four bit Synchronous MOD-N counter with Asynchronous reset • Write Verilog Code • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist Identify Critical pathVerify the functionality using Gate level netlist and compare the results at RTL and gate level netlist.
6.	a) Construct the schematic of CMOS inverter with load capacitance of 0.1pF and set

	the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following: i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and the time period of 20ns and plot the input voltage and output voltage of designed inverter? ii. From the simulation result compute tpHL, tpLH and td for all three geometrical settings of width? iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre layout simulations and compare the results.
7.	Capture the schematic of 2-input CMOS NOR gate having similar delay as that of CMOS inverter computed in experiment above. Verify the functionality of NOR gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.
8.	Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment above. Verify the functionality of NOR gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.
9.	Construct the schematic of the Boolean Expression Y= AB+CD+E using CMOS Logic. Verify the functionality of the expression find out the delay td for some combination of input vectors. Tabulate the results.
10.	a) Construct the schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measure the Unit Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB. b) Draw Layout of common source amplifier, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with prelayout simulations. Record the observations.
11.	a) Construct the schematic of two-stage operational amplifier and measure the following: i. Unity gain Bandwidth ii. dB Bandwidth iii. Gain Margin and phase margin with and without coupling capacitance iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality. v. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in part a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations and perform the comparative analysis.

Course Outcomes: At the end of the course, the students will be able to	
CO1	Analyze the Design and simulation of combinational and sequential digital circuits using Verilog HDL.
CO2	Analyzethe synthesis process of digital circuits using EDA tool.
CO3	Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist.
CO4	Design and simulate basic CMOS circuits like inverter, NOR gate and any Boolean expression .
CO5	Perform RTL_GDSII flow and understand the stages in ASIC design.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

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CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Laboratory	**Lab Conduction & Record**	**Evaluating each expt. for 10 marks**	**20**	**50**
	Laboratory Test -1	**50**	**15**	
	Laboratory Test -2	**50**	**15**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
4. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
5. Change of experiment is allowed only once and 15% of Marks allotted to the Conduction procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	-	2	-	3	-	-	-	-	-	1
CO2	2	-	2	-	3	-	-	-	-	-	1
CO3	2	-	2	-	3	-	-	-	-	-	1
CO4	2	-	2	-	3	-	-	-	-	-	1
CO5	2	-	2	-	3	-	-	-	-	-	1

Level 3- High, Level 2- Moderate, Level 1-Low

Semester-VI					
Verilog HDL Lab **Category: AEC-VI**					
Course Code	:	**B24EC681**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	0:0:2:0	SEE	:	50 Marks
Total Hours	:	30	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To understand FPGA Design flow for VLSI Chip Design.
2.	To understand the concept of Design and implementation of Advanced Digital System Design using Verilog HDL.
3.	To learning the Implementation of advanced digital circuits on FPGA boards.

Sl. No	**List of Experiments**
1	Write a Verilog description for the following combinational logic, verify the design using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. Structural modeling of Full adder using two half adders and OR Gate b. BCD to Excess-3 code converter
2	Write a Verilog description for the following Sequential Circuits, Verify the design using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. Mod-N counter b. Random sequence counter
3	Write a Verilog description for the following Sequential Circuits, Verify the design using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. SISO and PISO shift register b. Ring counter
4	Write a Verilog description for the following Digital Circuits, Verify the functionality using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. 4-Bit Ripple Carry Adder b. 4-Bit Linear Feedback shift register
5	Write a Verilog description for the following Digital Circuits, Verify the functionality using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. 4-bit Array Multiplication b. 4-bit Booth MultiplicatioN
6	Write a Verilog description to design a clock divider circuit that generates 1 /2, 1 /3 rd and 1 /4 th clock from a given input clock. Port the design to FPGA and validate the functionality using output device.
7	Interface a Stepper motor to FPGA and Write a Verilog description to control Stepper motor rotation
8	Interface a DAC to FPGA and Write a Verilog description to generate Square wave of frequency F KHz. Modify the code to down sample the frequency to F/2 KHz. Display the original and down sampled signals by connecting them to an output device.
9	Write a Verilog description to convert an analog input of a sensor to digital form and to display the same on a suitable display like set of simple LEDs like 7-Segment display digits.

Course Outcomes: At the end of the course, the students will be able to	
CO1	Familiarize with the EDA tool to write HDL programs to understand simulation and synthesis of digital design.
CO2	Design, Simulation and Synthesis of Combinational circuits using EDA tool
CO3	Design, Simulation and Synthesis of Sequential Circuits using EDA tool
CO4	Interfacing DAC to FPGA device to generate different waveforms using Verilog HDL.
CO5	Interfacing Stepper motor to FPGA device to count the number of rotations of a stepper motor.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

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CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Laboratory	**Lab Conduction & Record**	**Evaluating each expt. for 10 marks**	**20**	**50**
	Laboratory Test -1	**50**	**15**	
	Laboratory Test -2	**50**	**15**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
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CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	1	2	-	3	-	-	-	-	-	1
CO2	2	1	2	-	3	-	-	-	-	-	1
CO3	2	1	2	-	3	-	-	-	-	-	1
CO4	2	1	2	-	3	-	-	-	-	-	1
CO5	2	1	2	-	3	-	-	-	-	-	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-VI					
System Modeling using Simulink Lab **Category: AEC-VI**					
Course Code	:	**B24EC682**	CIE	:	50 Marks
Teaching Hours L:T :P:S	:	0:0:2:0	SEE	:	50 Marks
Total Hours	:	30	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To understand the basics of MATLAB Simulink used for engineering applications.
2.	To simulate the trigonometric functions and display of signals.
3.	To analyze the implementations of analog and digital systems using Simulink.
4.	To implement digital logic circuits using simulink and display the output.
5.	To simulation of the analog and digital communication systems using simulink.

Sl. No.	**List of the experiments**
1.	a) Generate the following signals using Simulink and display these signals on a single scope with separate inputs. i) Sinusoidal signal, ii) Square signal, iii) Sawtooth signal, and iv) Random signal b) Perform the following operations using simulink and display the output. i) y(t) = sin2t, ii) y(t) = $d(sin2t)\ dt$, iii)y(t) = $\int sin2t$
2.	Solve the second order differential equations shown below using Simulink and display the output. i) $d\ 2y\ dt2$ + 2 $dy\ dt$ + 5y = 1 ii) $d\ 2y\ dt2$ + 3 $dy\ dt$ + 4y = 5cos2t
3.	Design and realize the second order low pass and high pass RC filters using Simulink.
4.	Design a BCD adder and use Simulink to simulate and verify its operation.
5.	Design and Simulate the following using Simulink and verify its operation. a) 3−bit Up / Down Counter, b) 4−bit Ring Counter
6.	Design and simulate the 4x1 Multiplexer and 1x4 Demultiplexer using Simulink
7.	Find the step response of the following system functions given below, using Simulink. i) Continuous transfer function H(s) = 5(s+2) s(2s2+4s+3) ii) Discrete transfer function H(z) = z 2−1.2z+1 z 3−1.3z2+z−0.2
8.	Realize the FIR filter given by the impulse response h(n) = {0.08, 0.21,0.54, 0.86, 1, 0.86, 0.54, 0.21 0.08) using Simulink. Obtain the frequency response characteristics.
9.	Simulate the Amplitude Modulation and Demodulation using Simulink. Display the output signal and its spectrum.
10.	Simulate the modulation & demodulation of a random binary data stream using QPSK using Simulink. Display the output signal and its spectrum.
11.	Bit error rate (BER) improvement using Pulse Shaping on 16– QAM signal. (Use forward error correction (FEC) coding.)
12.	Adjacent and Co-Channel Interference using Simulink. • Use PSK-modulated signals to show the effects of adjacent and co-channel interference on a transmitted signal.

Reference Book:	
1.	Modeling and simulation of systems using MATLAB and Simulink by Devendra K. Chaturvedi

Course Outcomes: At the end of the course, the students will be able to	
CO1	Demonstrate the fundamentals of MATLAB and Simulink for solving basic engineering problems.
CO2	Generate, simulate and visualize trigonometric and time-varying signals using Simulink blocks.
CO3	Analyze and model analog and digital systems using appropriate Simulink tools and techniques.
CO4	Design and implement digital logic circuits in Simulink and interpret their output responses.
CO5	Simulate and evaluate the performance of analog and digital communication systems using Simulink models.

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SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

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CO3	3	2	3	-	2	-	-	-	-	-	1
CO4	3	3	2	-	2	-	-	-	-	-	1
CO5	3	3	2	2	2	-	-	-	-	-	1

Level 3 – High, Level 2 – Moderate, Level 1 -Low

Semester-VI					
Python Programming for Machine Learning Laboratory **Category : AEC-VI**					
Course Code	:	**B24EC683**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	0 : 0 : 2:0	SEE	:	50 Marks
Total Hours		30	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To become familiar with data and visualize univariate, bivariate, and multivariate data using statistical techniques and dimensionality reduction
2.	To understand various machine learning algorithms such as similarity-based learning, regression, decision trees, and clustering.
3.	To familiarize with learning theories, probability-based models and developing the skills required for decision-making in dynamic environments.

Sl. No	**List of Experiments**
1	Develop a program to create histograms for all numerical features and analyze the distribution of each feature. Generate box plots for all numerical features and identify any outliers. Use California Housing dataset.
2	Develop a program to Compute the correlation matrix to understand the relationships between pairs of features. Visualize the correlation matrix using a heatmap to know which variables have strong positive/negative correlations. Create a pair plot to visualize pairwise relationships between features. Use California Housing dataset.
3	Develop a program to implement Principal Component Analysis (PCA) for reducing the dimensionalityof the Iris dataset from 4 features to 2.
4	For a given set of training data examples stored in a .CSV file, implement and demonstrate the Find-S algorithm to output a description of the set of all hypotheses consistent with the training examples.
5	Develop a program to implement k-Nearest Neighbour algorithm to classify the randomly generated 100 values of x in the range of [0,1]. Perform the following based on dataset generated. 1. Label the first 50 points {x1,……,x50} as follows: if (xi ≤ 0.5), then xi ∈ Class1, else xi ∈ Class1 2. Classify the remaining points, x51,……,x100 using KNN. Perform this for k=1,2,3,4,5,20,30
6	Implement the non-parametric Locally Weighted Regression algorithm in order to fit data points. Select appropriate data set for your experiment and draw graphs
7	Develop a program to demonstrate the working of Linear Regression and Polynomial Regression. Use Boston Housing Dataset for Linear Regression and Auto MPG Dataset (for vehicle fuel efficiency prediction) for Polynomial Regression.
8	Develop a program to demonstrate the working of the decision tree algorithm. Use Breast Cancer Data set for building the decision tree and apply this knowledge to classify a new sample.
9	Develop a program to implement the Naive Bayesian classifier considering Olivetti Face Data set for training. Compute the accuracy of the classifier, considering a few test data sets.
10	Develop a program to implement k-means clustering using Wisconsin Breast Cancer data set and visualize the clustering result.
Course Outcomes: At the end of the course, the students will be able to	
CO1	Illustrate the principles of multivariate data and apply dimensionality reduction techniques.
CO2	Demonstrate similarity-based learning methods and perform regression analysis.
CO3	Develop decision trees for classification and regression problems, and Bayesian models for probabilistic learning.
CO4	Implement the clustering algorithms to share computing resources.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Laboratory	Lab Conduction & Record	Evaluating each expt. for 10 marks	20	50
	Laboratory Test -1	50	15	
	Laboratory Test -2	50	15	
SEE	Semester End Examination	100	50	50
Total Marks				100

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
4. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
5. Change of experiment is allowed only once and 15% of Marks allotted to theConduction procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	1	2	-	2	-	-	-	-	-	1
CO2	2	1	2	-	2	-	-	-	-	-	1
CO3	2	1	2	-	2	-	-	-	-	-	1
CO4	2	1	2	-	2	-	-	-	-	-	1
CO5	2	1	2	-	2	-	-	-	-	-	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-VI					
Fiber Optic Communication Lab **Category : AEC-VI**					
Course Code	:	**B24EC684**	CIE	:	50 Marks
Teaching Hours L:T:P:S	:	0:0:2:0	SEE	:	50 Marks
Total Hours	:	30	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Learning Objective is	
1.	To understand the concept of optical communication.
2.	To understand and study about the concept of optical communication devices.
3.	To understand the concept of optical communication device Characteristics.
4.	To understand the concept of optical communication devices parameters.

Sl. No	**List of Experiments**
1.	Measurement of numerical aperture of a fiber after preparing the fiber ends.
2.	Study of losses in optical fiber
3.	Setting up of fiber optic digital link
4.	Preparation of splice joint and measurement of splice loss.
5.	Power vs. current (P-I) characteristics and measure slope efficiency of laser diode.
6.	Voltage vs. current(V-I) characteristics of laser diode
7.	Power vs. current (P-I)characteristics and measure slope efficiency of LED
8.	Voltage vs. current(V-I) characteristics of LED
9.	Characteristics of photodiode and measure the responsivity
10.	Characteristics of avalanche photodiode [APD] and measure the responsivity.
11.	Measurement of fiber characteristics, fiber damage and splice loss/connector loss by OTDR 6

Course Outcomes: At the end of the course, the students will be able to	
CO1	Express the principles and operation of fibre optic communication system
CO2	Analyze with use of various optical components constituting optical fiber links
CO3	Calculate different kind of losses and signal distortion
CO4	Design an optical fiber link with encapsulation of different system components.
CO5	Express the measurement techniques for performance parameters of optical fiber

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Laboratory	**Lab Conduction & Record**	**Evaluating each expt. for 10 marks**	**20**	**50**
	Laboratory Test -1	**50**	**15**	
	Laboratory Test -2	**50**	**15**	
SEE	**Semester End Examination**	**100**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
4. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
5. Change of experiment is allowed only once and 15% of Marks allotted to the Conduction procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	1	2	-	3	-	-	-	-	-	1
CO2	2	1	2	-	3	-	-	-	-	-	1
CO3	2	1	2	-	3	-	-	-	-	-	1
CO4	2	1	2	-	3	-	-	-	-	-	1
CO5	2	1	2	-	3	-	-	-	-	-	1

Level 3- High, Level 2- Moderate, Level 1-Low

MOOGAMBIGAI CHARITABLE AND EDUCATIONAL TRUST

Rajarajeswari College of Engineering

(An Autonomous Institution under Visvesvaraya Technological University, Belagavi)
#14, Ramohalli Cross, Kumbalagodu, Mysore Road, Bengaluru–560074

Common Courses

V & VI Semester

UG – B.E (2024 Scheme)

INDEX

Sl. No.	Course Code	Course Title	Page No.
1.	B24BEK507	Biology for Engineers	1
2.	B24ESK510	Environmental Science and E-Waste Management	3
3.	B24RMK606	Research Methodology and IPR	5
4.	B24PRJ607	Capstone Project work: Phase I	7
5.	B24IKK610	Indian Knowledge System	12
6.	B24NCK591/691	National Service Scheme (NSS)	14
7.	B24NCK592/692	National Cadet Corps (NCC)	16
8.	B24NCK593/693	Physical Education (PE)	17
9.	B24NCK594/694	Yoga	24
10.	B24NCK595/695	Music	32

Semester-V					
Biology for Engineers **Category: BSC** **(Common to All)**					
Course Code	:	**B24BEK507**	CIE	:	50 Marks
Teaching Hours L : T : P : S	:	2:0:0:2	SEE	:	50 Marks
Total Hours	:	30	Total	:	100 Marks
Credits	:	2	SEE Duration	:	2 Hrs

Course Learning Objective is	
1.	To familiarize the students with the basic biological concepts and their engineering applications.
2.	To enable the students with an understanding of biodesign principles to create novel devices and structures.
3.	To provide the students an appreciation of how biological systems can be re-designed as substitute products for natural systems.
4.	To motivate the students to develop interdisciplinary vision of biological engineering.

Module– 1	**No. of Hours**
Introduction to Biology: The cell: the basic unit of life, Structure and functions of a cell. The Plant Cell and animal cell, Prokaryotic and Eukaryotic cell, Stem cells and their application. **Biomolecules:** Properties and functions of Carbohydrates, Nucleic acids, proteins, lipids. Importance of special biomolecules; Enzymes (Classification (with one example each), Properties and functions), vitamins and hormones.	6
Module– 2	**No. of Hours**
Application of Biomolecules: Carbohydrates in cellulose-based water filters production, PHA and PLA in bio plastics production, Nucleic acids in vaccines and diagnosis, Proteins in food production.	6
Module– 3	**No. of Hours**
Adaptation of Anatomical Principles for Bioengineering Design: Brain as a CPU system. Robotic arms for prosthetics. Engineering solutions for Parkinson's disease. Eye as a Camera system, bionic eye. Heart as a pump system, pace makers, defibrillators. Lungs as purification system, Heart-lung machine. Kidney as a filtration system, dialysis systems.	6
Module– 4	**No. of Hours**
Nature-Bioinspired Materials and Mechanisms: Echolocation, Photosynthesis. Bird flying, Lotus leaf effect, Shark skin, Kingfisher beak. Human Blood substitutes - hemoglobin-based oxygen carriers (HBOCs) and perflourocarbons (PFCs).	6
Module– 5	**No. of Hours**
Trends in Bioengineering: DNA origami and Biocomputing, Bioprinting techniques and materials. Bioimaging and Artificial Intelligence for disease diagnosis. Bioconcrete. Biomining.	6

Course Outcomes: At the end of the course, the students will be able to	
CO1	Elucidate the basic biological concepts via relevant industrial applications and case studies.
CO2	Evaluate the principles of design and development, for exploring novel bioengineering projects.
CO3	Corroborate the concepts of biomimetics for specific requirements.
CO4	Think critically towards exploring innovative biobased solutions for socially relevant problems.

Text Books	
1.	Biology for Engineers, Rajendra Singh C and Rathnakar Rao N, Rajendra Singh C and Rathnakar Rao N Publishing, Bengaluru, 2023.
2.	Human Physiology, Stuart Fox, Krista Rompolski, McGraw-Hill eBook. 16th Edition, 2022

Web links and Video Lectures (E-Resources)

- https://nptel.ac.in/courses/121106008
- https://freevideolectures.com/course/4877/nptel-biology-engineers-other-non-biologists
  https://ocw.mit.edu/courses/20-020-introduction-to-biological-engineering-design-spring-2009

• https://ocw.mit.edu/courses/20-010j-introduction-to-bioengineering-be-010j-spring-2006 • https://www.coursera.org/courses?query=biology	
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning	
1.	Group Discussion of Case studies.
2.	Model Making and seminar/poster presentations.
3.	Design of novel device/equipment like Cellulose-based water filters, Filtration system.

ASSESSMENT DETAILS (BOTH CIE AND SEE)

The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage. To qualify and become eligible to appear for SEE, in the CIE, a student must score at least 40% of 50 marks, i.e., 20 marks. To pass the SEE, a student must score at least 35% of 50 marks, i.e., 18 marks. Notwithstanding the above, a student is considered to have passed the course, provided the combined total of CIE and SEE is at least 40 out of 100 marks.

CONTINUOUS INTERNAL EVALUATION (CIE):

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment1**	**50**	**30 (Average of Best two Assessments)**	**50**
	Internal Assessment2	**50**		
	Internal Assessment3	**50**		
AAT	**Any Two Assessments as per Regulations**	**20**	**20**	
SEE	**Semester End Examination**	**50**	**50**	**50**
Total Marks				**100**

SEMESTER END EXAMINATION (SEE):

1. The Question paper shall be set for 50 marks and duration of SEE is 2 Hours.
2. Two questions of 10 marks (with minimum two sub questions) from each module with internal choice.
3. Students should answer five full questions, selecting one full question from each module.
4. Mention COs, POs, Bloom's Taxonomy levels in the question paper.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO8	PO11
CO1	1	-	-	-	-	1	1	-	1	1	1
CO2	1	-	-	-	-	1	-	1	-	1	1
CO3	1	-	-	-	-	1	-	1	-	1	1
CO4	1	-	-	-	-	1	2	-	2	1	1
CO5	1	-	-	-	-	1	2	2	1	2	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-V					
Environmental Science and E-Waste Management **Category: NCMC** **(Common to All)**					
Course Code	:	**B24ESK510**	CIE	:	100 Marks
Teaching Hours L : T : P : S	:	2:0:0:0	SEE	:	-
Total Hours/Semester	:	30	Total	:	100 Marks
Credits	:	PP	SEE Duration	:	-

Course Learning Objective is	
1.	To identify the major challenges of environment issues.
2.	To develop skills, critical thinking and demonstrate socio-economic skills for Environmental protection.
3.	To analyze the impact of issues w. r. t. waste management.

Module– 1	**No. of Hours**
Ecosystem and Sustainability: Ecosystems: Structure of Ecosystem, Types: Forest, Desert, Wetlands, Riverine, Oceanic ecosystems. **Sustainability:** 17SDG targets and possible actions.	6
Module– 2	**No. of Hours**
Natural Resources and Energy: Natural Resources: Water resources-Availability & Quality aspects, Water borne diseases & water induced diseases, Fluoride problem in drinking water. **Energy:** Different types of energy, Conventional sources & Non-Conventional sources of energy, solar energy. Wind energy, Hydrogen as an alternative energy.	6
Module– 3	**No. of Hours**
Environmental Pollution: Water Pollution, Noise pollution, Air pollution (Sources, Impacts, Preventive measures and public Health Aspects. **Global Environmental Concerns (Concept, policies and case-studies):** Ground water depletion/recharging, Climate Change; Acid Rain; Ozone Depletion; Radon and Fluoride problem in drinking water; Resettlement and rehabilitation of people, Environmental Toxicology.	6
Module– 4	**No. of Hours**
Waste management: Solid Waste Management, types and sources, functional elements of SWM, Biomedical Waste Management-Sources, Characteristics. **Environmental Legislation:** Solid Waste Management Rules, 2016, Biomedical Waste Management Rules, 2016.	6
Module– 5	**No. of Hours**
E-Waste Management: E-waste; composition and generation. Global context in e-waste; E-Waste pollutants, E-waste hazardous properties, Effects of pollutant (E-waste) on human health and surrounding environment, domestic e-waste disposal, Basic principles of E waste management, Component of E Waste management. E-waste (Management and Handling) Rules, 2011; and E-waste (Management) Rules, 2022-Salient Features and its implications.	6

Course Outcomes: At the end of the course, the students will be able to	
CO1	Comprehend the principles of ecology and environmental issues pertaining to air, land and water on a global scale.
CO2	Acquire observation skills for solving problems related to the environment.
CO3	Conduct survey to describe the realities of waste management system.

Text Books	
1.	S M Prakash, "Environmental Studies" 3rd Edition, Elite Publishing House, Mangalore, 2018.
2.	Hester R.E., and Harrison R.M, Electronic Waste Management. Science, 2009.

Reference Text Books	
1.	Benny Joseph (2005), "Environmental Studies" , Tata McGraw – Hill Publishing Company Limited.
2.	Johri R., E-waste: implications, regulations, and management in India and current global best practices, TERI Press, New Delhi.

Web links and Video Lectures (e-Resources):	
1.	https://www.youtube.com/playlist?list=PLXTQoJ3yDR1Tp9O8R7RZGmm_GdheHqM2w
3.	https://sdgs.un.org/goals
4.	https://kspcb.karnataka.gov.in/waste-management/biomedical-waste
5.	E Waste (Management) Rules, 2022: https://kspcb.karnataka.gov.in/sites/default/files/inlinefiles/ E%20Waste%20%28Management%29%20Rules%2C%202022.pdf

ASSESSMENT DETAILS (CIE only)

The weightage of Continuous Internal Evaluation (CIE) is 100%. The minimum passing mark for the CIE is 40% of the maximum marks (40 marks out of 100).

CONTINUOUS INTERNAL EVALUATION (MCQs)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	**Internal Assessment-1**	**50**	**50 (Average of Best two Assessments)**	**100**
	Internal Assessment-2	**50**		
	Internal Assessment-3	**50**		
AAT	**Two Assessments as per Regulations**	**50**	**50**	
Total Marks				**100**

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	1	0	0	0	0	3	2	0	0	0	0
CO2	0	0	0	0	0	1	1	0	0	0	1
CO3	0	0	0	0	0	2	2	0	0	0	2

Level 3 - High, Level 2 - Moderate, Level 1 - Low

Semester-V					
Research Methodology & IPR (RMIPR) **Category: AEC**					
Course Code	:	**B24RMK606**	CIE	:	50 Marks
Teaching Hours L:T: P : S	:	1 : 0 : 0 : 3	SEE	:	50 Marks
Total Hours/Semester	:	15	Total	:	100 Marks
Credits	:	1	SEE Duration	:	1 Hours

Course Learning Objective is	
1.	To understand the fundamentals of research, types of research methodologies, and ethical practices involved in engineering research.
2.	To develop the ability to conduct effective literature review, technical reading, and identify research gaps for problem formulation.
3.	To design research methodologies, apply appropriate sampling techniques, and perform data collection and hypothesis testing.
4.	To analyze, interpret, and present research findings through structured technical reports and research papers using standard tools and formats.
5.	To understand Intellectual Property Rights (IPR), patenting processes, and their role in innovation, society, and sustainable development.

Module – 1	**No. of Hours**
Introduction to Research & Research Methodology: Meaning, Objectives of Engg. Research & Characteristics of good research, Research Methods v/s Research Methodology, Types of engineering research, Descriptive v/s Analytical, Applied v/s Fundamental, Quantitative v/s Qualitative, Conceptual v/s Empirical, Research, Criteria of good research, Developing a research plan, Ethics & plagiarism in Engineering Research with Research Practice for different types of Research Misconducts, Case Study and Practice Sessions	3
Module – 2	**No. of Hours**
Literature Review and Technical Reading: What is literature review or survey, New & Existing Knowledge, Bibliographic Databases, Search Engines, Google & Google Scholar, Effective Search, Conceptualizing Research Reviews, Gaps in research, Critical and Creative Reading, Taking Notes While Reading, Defining research problems, Datasheets, Importance of literature review in defining a problem, Primary and secondary sources of info - Review articles, treatise, monographs, papers from conferences & journals, case-studies, reports, patents, web and net searching ; Identifying gap areas from literature review, Citations, Acknowledgments, Case Studies and Practice sessions.	3
Module – 3	**No. of Hours**
Research Design and Methods: Research design, Basic Principles, Need for research design, Features of good design, Development of Models, Developing a research plan, Exploration, Description, Diagnosis, Simulation and Experimentations, Determining experimental and sample designs, Sampling design, Steps in sampling design, Characteristics of a good sample design, Types of sample designs, Measurement and scaling techniques, Methods of data collection, Collection of primary & secondary data, Data collection instruments, Hypothesis - Basic Concepts, Testing of hypotheses, flow diagram for hypotheses testing, Case Study and Practice Sessions.	3
Module – 4	**No. of Hours**
Technical Report & Paper Writing: Interpretation and report writing, Techniques of interpretations, Structure and components of scientific reports, Different steps in the report preparation – Layout, organization, structure and language of the report, Illustrations and tables with result analysis (simulation or experimentation), Types of reports, technical reports, project reports (mini & major) and research thesis, Research tools for writing, Conclusions, Future works, Flow of a research article, Research paper writing for conference & journals, text-books, Case Study and Practice Sessions.	3
Module – 5	**No. of Hours**
IPRs & Copyrights: Intellectual Property, what are patents & copyrights in IP? Role of IP in the Economic and Cultural Development of the Society, IP Governance, Invention and Creativity, Importance and Protection of Intellectual Property Rights (IPRs), A brief summary of - Patents, Monographs, Copyrights ©, Registered Firms ®, Trademarks ™, Industrial Designs (Design Patent,	3

Utility Patent, Granted Patent, Commercialized Patent) – Indian &Foreign Patents, Steps in Patenting — Application and Procedures with Searches, Case Study and Practice Sessions.	

Course Outcomes: At the end of the course, the students will be able to	
CO1	Explain research fundamentals, methodologies, and ethical practices in engineering research.
CO2	Perform literature review, identify research gaps, and formulate research problems.
CO3	Design research experiments, collect data, and apply hypothesis testing methods.
CO4	Analyze results and prepare technical reports and research papers.
CO5	Apply IPR concepts including patents, copyrights, and trademarks in research and innovation.

Research Papers & Technical References (Web-links & Video Resources)

- IEEE Xplore – https://ieeexplore.ieee.org
- Scopus – https://www.scopus.com
- Science Direct – https://www.sciencedirect.com
- Google Scholar – https://scholar.google.com
- Research Gate – https://www.researchgate.net

ASSESSMENT DETAILS (BOTH CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (MCQs)

CIE	Type of Assessment	Max. Marks	Max. Marks Scaling Down to	Total Marks
Theory	Internal Assessment-1	50	30 (Average of Best two Assessments)	50
	Internal Assessment-2	50		
	Internal Assessment-3	50		
AAT	Two Assessments as per regulations	20	20	
SEE	Semester End Examination	50		50
Total Marks				100

SEMESTER END EXAMINATION (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is 01 hour. The student has to secure a minimum of 35% of the maximum marks meant for SEE.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	-	1	-	-	2	-	-	-	2
CO2	3	3	-	2	1	-	1	1	1	-	2
CO3	2	3	3	3	2	-	1	2	-	-	2
CO4	2	2	3	3	3	-	1	2	3	1	2
CO5	1	1	-	-	1	3	3	1	2	2	2

L = Low (**1**), M = Medium (**2**), H = High (**3**) - Blank = No significant mapping correlation levels

Semester - VI					
Capstone Project Work: Phase - I **Category: SDC**					
Course Code	:	**B24PRJ607**	CIE	:	100 Marks
Teaching Hours L:T:P:S	:	0:0:4:0	SEE	:	-
Total Hours	:	60	Total	:	100 Marks
Credits	:	2	SEE Duration	:	-

Capstone Project: Phase -I and Phase - II

The Capstone project is a comprehensive, year-long project carried out in two phases during **6th and 7th** semesters of the undergraduate program. It integrates knowledge and skills acquired from multiple courses and disciplines to address a complex, real-world problem.

This project provides students with an opportunity to apply scientific principles, engineering methodologies, and technological tools to conceive, design, implement and evaluate an engineering solution.

It serves as a culminating academic experience to demonstrate program outcomes, including problem-solving ability, teamwork, communication skills, and practical application of engineering principles. Students can take up project individually or in a group not exceeding 4 students. The group may have students from the same discipline and drawn from different disciplines.

Types of Capstone Projects: Capstone projects undertaken for one year may fall into one or more of the following categories:

a) Research-Oriented Projects :
   • Focus on investigating new concepts, theories, or technologies.
   • Aim to generate new knowledge or contribute to academic research.
b) Experimental/Analytical Projects
   • Based on laboratory or field experiments to validate a hypothesis or study a phenomenon.
   Simulation/ Modelling Projects
   • Including detailed data collection, analysis, and interpretation.
   • Use computational tools to model, simulate, and predict system behavior.
   • Reduce the need for physical prototyping in the initial stages.
c) Industrial/Industry-Sponsored Projects
   • Carried out in collaboration with an industry partner.
   • Address real-world engineering problems faced by the organization.
d) Interdisciplinary/Multidisciplinary Projects
   • Combine knowledge and techniques from multiple engineering domains or other fields such as management, medicine, or environmental sciences.
e) Entrepreneurial/Innovation Projects
   • Focus on product or service innovation with potential for commercialization.

- Phase I Evaluation: Capstone Project Phase-I shall have only Continuous Internal Evaluation (CIE).
- In case disciplinary capstone project, the CIE shall be conducted by the Departmental Project Review Committee, which consists of a Senior Professor, the Project Guide, and one additional faculty member appointed by the principal for projects within the parent discipline.
- For Interdisciplinary Projects, the Project Review Committee will consist of one Senior Professor, the department and interdepartmental Project Guides and one faculty member from a department related to the interdisciplinary project. The committee members are appointed by the principal of the college.
- Phase I evaluation shall be based on rubrics designed to measure graduate attributes defined by NBA. Successful completion of Phase-I allows the student to proceed to Phase-II.
- Phase II Evaluation: CIE of Phase shall be evaluated as indicated with phase -I evaluation. The SEE shall be conducted by two examiners. The assessment shall be based on rubrics designed to measure graduate attributes.

Review #	**Agenda**	**Assessment**	**Review Assessment Weightage**
Review1	Project Synopsis / Proposal Evaluation	Rubric R1	15
Review2	Mid-Term Project Evaluation	Rubric R2	30
Review3	End Semester Project Evaluation	Rubric R3	30
Review4	Project Report Evaluation	Rubric R4	15
Review5	Evaluation by Guide	Rubric R5	10
Continuous Internal Evaluation (CIE)			100
Total Marks			100

Rubric #R1: Project Synopsis / Proposal Evaluation Maximum Marks: 15

		Excellent (5 Marks)	Good (4 Marks)	Average (3 Marks)	Acceptable (2 Marks)	Unacceptable (1 Marks)
a	**Identification of Problem Domain and Detailed Analysis**	Detailed and extensive explanation of the purpose and need of the project	Good explanation of the purpose and need of the project	Average explanation of the purpose and need of the project	Moderate explanation of the purpose and need of the project	Minimal explanation of the purpose and need of the project
b	**Study of the Existing Systems and Feasibility of Project Proposal**	Detailed and extensive explanation of the specifications and the limitations of the existing systems	Collects a great deal of information and good study of the existing systems	Moderate study of the existing systems; collects some basic information	Explanation of the specifications and the limitations of the existing systems not very satisfactory; limited information	Minimal explanation of the specifications and the limitations of the existing systems; incomplete information
c	**Objectives and Methodology of the Proposed Work**	All objectives of the proposed work are well defined; Steps to be followed to solve the defined problem are clearly specified	Good justification to the objectives; Methodology to be followed is specified but detailing is not done	Incomplete justification to the objectives proposed; Steps are mentioned but unclear; without justification to objectives	Only Some objectives of the proposed work are well defined; Steps to be followed to solve the defined problem are not specified properly	Objectives of the proposed work are either not identified or not well defined; Incomplete and improper specification

Rubric #R2: Mid-term Project Evaluation Maximum Marks: 30

Level of Achievement						
		Excellent(10)	**Good (8)**	**Average(6)**	**Acceptable(4)**	**Unacceptable (2)**
a	**Design Methodology**	• Division of problem in to modules and good selection of computing framework. • Appropriate design methodology and properly justification.	• Division of problem into modules and good selection of computing frame work. • Design methodology not properly justified.	• Division of problem into modules but in appropriate selection of computing framework. • Design methodology not defined properly.	• Partial division of problem into modules and inappropriate selection of computing framework. • Design methodology not defined properly.	• Modular approach not adopted. • Design methodology not defined.
b	**Planning of Project Work and Team Structure**	• Time frame properly specified and being followed. • Appropriate distribution of project work.	• Time frame properly specified and being followed. • Distribution of project work inappropriate.	• Time frame properly specified, but not being followed. • Distribution of project work un-even.	• Time frame properly specified, but not being followed. • Un-even distribution of Project work and no synchronization.	• Time frame not properly specified. • In-appropriate distribution of project work.

c	**Demonstration and Presentation**	• Objectives achieved as per time frame. • Contents of presentations are appropriate and well arranged. • Proper eye contact with audience and clear voice with good spoken language.	• Objectives achieved as per time frame • Contents of presentations are appropriate but not well arranged Satisfactory demonstration, clear voice with good spoken language but eye contact not proper	• Objectives achieved as per time frame. • Contents of presentations are appropriate but not well arranged. • Presentation not satisfactory and average demonstration	• Objectives not achieved as per time frame. • Contents of presentations are not appropriate. • Eye contact with few people and unclear voice.	• No objectives achieved. • Contents of Presentations are not appropriate and not well delivered. • Poor delivery of presentation.

Rubric #R3: End Semester Internal Project Evaluation Maximum Marks: 30

		Excellent(10)	Good (8)	Average(6)	Acceptable(4)	Unacceptable (2)
a	**Incorporation of Suggestions**	Changes are made as per modifications suggested during midterm evaluation and new innovations added	Changes are made as per modifications suggested during mid-term evaluation and good justification	All major changes are made as per modifications suggested during midterm evaluation	Few changes are made as per modifications suggested during midterm evaluation	Suggestions during mid-term evaluation are not incorporated
b	**Project Demonstration**	• All defined objectives are achieved. • Each module working well and properly demonstrated. • All modules of project are well integrated and system working is accurate.	• All defined objectives are achieved. • Each module working well and properly demonstrated. • Integration of all modules not done and system working is not very satisfactory.	• All defined objectives are achieved. • Modules are working well in isolation and properly demonstrated. • Modules of project are not properly integrated.	• Some of the defined objectives are achieved. • Modules are working well in isolation and properly demonstrated • Modules of project are not properly integrated.	• Defined objectives are not achieved. • Modules are not in proper working form that further leads to failure of integrated system.
c	**Presentation**	• Contents of presentations are appropriate and well delivered. • Proper eye contact with audience and clear voice with good spoken language	• Contents of presentations are appropriate and well delivered. • Clear voice with good spoken language but less eye contact with audience	• Contents of presentations are appropriate but not well delivered . • Eye contact with few people and unclear voice	• Contents of presentations are not appropriate. • Eye contact with few people and unclear voice	• Contents of presentations are not appropriate and not well delivered . • Poor delivery of presentation

Rubric #R4: Project Report Evaluation Maximum Marks: 15

Level of Achievement						
		Excellent(5)	**Good (4)**	**Average(3)**	**Acceptable(2)**	**Unacceptable (1)**
a	**Project Report**	• Project report is according to the specified format. • References and citations are appropriate and well mentioned.	• Project report is according to the specified format. • References and citations are appropriate but not mentioned well.	• Project report is according to the specified format but some mistakes. • In-sufficient references and citations.	• Project report is not fully according to the specified format. • In-sufficient references and citations	• Project report not prepared according to the specified format. • References and citations are not appropriate
b	**Description of Concepts and Technical Details**	• Complete explanation of the key concepts. • Strong description of the technical requirements of the project.	• Complete explanation of the key concepts. • In-sufficient description of the technical requirements of the project.	• Complete explanation of the key concepts but little relevance to literature. • In-sufficient description of the technical requirements of the project.	• All key concepts are not explained and very little relevant to literature. • In-sufficient description of the technical requirements of the Project.	• Inappropriate explanation of the key concepts. • Poor description of the technical requirements of the project.
c	**Conclusion and Discussion**	• Results are presented in very appropriate manner • Project work is well summarized and concluded. • Future extensions in the project are well specified.	• Results are presented in good manner. • Project work summary and conclusion not very appropriate. • Future extensions in the project are specified.	• Results presented are not much Satisfactory. • Project work summary and conclusion not very appropriate. • Future extensions in the project are specified.	• Results presented are not much satisfactory. • Project work summary and conclusion not very appropriate. • Future extensions in the project are not specified.	• Results are not presented properly. • Project work is not summarized and concluded. • Future extensions in the project are not specified.

Rubric #R5: Evaluation by Guide Maximum Marks: 10

Level of Achievement				
		Excellent (5)	**Satisfactory(3)**	**Unsatisfactory(2)**
a	**Self-Motivation, Determination and Regularity**	• Approaches the project with self-motivation and follows it through to completion. • Reports to the guide regularly and consistent in work.	• Completes the project but sometimes lacks self-motivation. • Reports to the guide but lacks consistency	• Lacks self-motivation and determination. • Irregular in attendance and in consistent in work.
b	**Working with in a Team & Technical Knowledge and Awareness related to the Project**	• Collaborates and communicates in a group situation and integrates the views of others. • Extensive knowledge related to the project.	• Exchanges some views but requires guidance to collaborate with others. • Fair knowledge related to the project	• Makes little or no attempt to collaborate in a group situation. • Lack sufficient knowledge.

Semester-VI					
Indian Knowledge Systems **Category: HSMC** **(Common to All)**					
Course Code	:	**B24IKK610**	CIE	:	100 Marks
Teaching Hours L:T:P:S	:	1:0:0:0	SEE	:	-
Total Hours/Semester	:	15	Total	:	100 Marks
Credits	:	PP	SEE Duration	:	-

Course Learning Objective is	
1.	To facilitate the students with the concepts of Indian traditional knowledge and to make them understand the Importance of roots of knowledge system.
2.	To make the students understand the traditional knowledge and analyse it and apply it to their day-to-day life.

Module– 1	**No. of Hours**
Introduction to Indian Knowledge Systems (IKS): Overview, Vedic Corpus, Philosophy, Character scope and importance, traditional knowledge vis-a-vis indigenous knowledge, traditional knowledge vs. western knowledge.	5
Module– 2	**No. of Hours**
Traditional Knowledge in Humanities and Sciences: Lingistics, Number and measurements-Mathematics, Chemistry, Physics, Art, Astronomy, Astrology, Crafts and Trade in India and Engineering and Technology.	5
Module– 3	**No. of Hours**
Traditional Knowledge in Professional domain: Town planning and architecture-Construction, Health, wellness and Psychology-Medicine, Agriculture, Governance and public administration, United Nations Sustainable development goals.	5

Course Outcomes: At the end of the course, the students will be able to	
CO1	Provide an overview of the concept of the Indian Knowledge System and its importance.
CO2	Appreciate the need and importance of protecting traditional knowledge.
CO3	Recognize the relevance of Traditional knowledge in different domains.
CO4	Establish the significance of Indian Knowledge systems in the contemporary world.

Text Books	
1.	Introduction to Indian Knowledge System- concepts and applications, B Mahadevan, Vinayak Rajat Bhat, Nagendra Pavana R N, 2022, PHI Learning Private Ltd, ISBN-978-93- 91818-21-0
2.	Traditional Knowledge System in India, Amit Jha, 2009, Atlantic Publishers and Distributors (P) Ltd., ISBN-13: 978-8126912230,
3	Knowledge Traditions and Practices of India, Kapil Kapoor, Avadesh Kumar Singh, Vol. 1, 2005, DK Print World (P) Ltd., ISBN 81-246-0334,

ASSESSMENT DETAILS (CIE only)
The weightage of Continuous Internal Evaluation (CIE) is 100%. The minimum passing mark for the CIE is 40% of the maximum marks (40 marks out of 100).

CONTINUOUS INTERNAL EVALUATION (MCQs)

CIE	Type of Assessment	Max. Marks	Max. Marks	Total Marks
Theory	Internal Assessment-1	50	100 (Sum of Best two Assessments)	100
	Internal Assessment-2	50		
	Internal Assessment-3	50		
Total Marks				**100**

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	1	0	0	0	0	3	2	0	0	0	0
CO2	0	0	0	0	0	1	1	0	0	0	1
CO3	0	0	0	0	0	2	2	0	0	0	2

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-V & VI					
NATIONAL SERVICE SCHEME (NSS) **Category: NCMC**					
Course Code	:	B24NCK591/691	CIE	:	100 Marks
Teaching Hours L : T : P	:	1:0:0	SEE	:	---
Total Hours	:	50	Total	:	100 Marks
Credits	:	--	SEE Duration	:	--

Course Objectives	
1.	Understand the community in which they work
2.	Identify the needs and problems of the community and involve the min problem-solving
3.	Develop among themselves a sense of social & civic responsibility & utilize their knowledge in finding practical solutions to individual and community problems
4.	Develop competence required for group-living and sharing of responsibilities & gain skills in mobilizing community participation to acquire leadership qualities and democratic attitudes
5.	Develop capacity to meet emergencies and natural disasters & practice national integration and social harmony

CONTENT	**No. of Hours**
1. Organic farming, Indian Agriculture (Past, Present and Future) Connectivity for marketing. 2. Waste management–Public, Private and Govt. organization. 3. Setting of the information imparting club for women leading to contribution in social and economic issues. 4. Water conservation techniques–Role of different take holders–Implementation. 5. Preparing an actionable business proposal for enhancing the village income and approach for implementation. 6. Helping local schools to achieve good results and enhance their enrolment in Higher/ technical/ vocational education. 7. Developing Sustainable Water management system for rural areas and implementation approaches. 8. Contribution to any national level initiative of Government of India.Digital India, Skill India, Swachh Bharat, Atmanirbhar Bharath, Make in India, Mudra scheme, Skill development programs etc. 9. Spreading public awareness under rural outreach programs.(minimum 5 programs). 10. Social connect and responsibilities. 11. Plantation and adoption of plants. Know your plants. 12. Organize National integration and social harmony events/ workshops / seminars. (Minimum 02 programs). 13. Govt. school Rejuvenation and helping them to achieve good infrastructure. **NOTE:** Students have to take up any one activity on the above said topics and have to prepare content for awareness and technical contents for implementation of the projects and have to present strategies for implementation of the same. Compulsorily students have to attend one camp. CIE will be evaluated based on their presentation, approach and implementation strategies.	50

Course Outcomes: After completing the course, the students will be able to	
CO1	Understand the importance of his/her responsibilities towards society.
CO2	Analyze the environmental and societal problems/issues and will be able to design solutions for the same.
CO3	Evaluate the existing system and to propose practical solutions for the same for sustainable development.
CO4	Implement government or self-driven projects effectively in the field.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO12
CO1	3	2	-	-	3	-	-	-	-	-	-
CO2	3	2	-	-	3	-	-	-	-	-	-
CO3	3	2	-	-	3	-	-	-	-	-	-
CO4	3	2	-	-	3	-	-	-	-	-	-

Level 3- Highly Mapped, Level 2-Moderately Mapped, Level 1-Low Mapped, Level 0- Not Mapped

SEMESTER-V & VI					
NATIONAL CADET CORPS (NCC) **Category: NCMC**					
Course Code	:	B24NCK592/692	CIE	:	100 Marks
Teaching Hours L : T : P	:	1:0:0	SEE	:	--
Total Hours	:	50	Total	:	100 Marks
Credits	:	--	SEE Duration	:	--

Course Objectives	
1.	To develop character, camaraderie, discipline, secular outlook, the spirit of adventure, sportsman spirit, and ideals of selfless service amongst cadets by working in teams, honing qualities such as self-discipline, self-confidence, self-reliance, and dignity of labour in the cadets.
2.	To create a pool of organized, trained, and motivated youth with leadership qualities from all walks of life, who will serve the Nation regardless of which career they choose
3.	To provide a conducive environment to motivate young Indians to choose the Armed Forces as a career

Content	No. of Hours
Unit 1. Personality Development: Group Discussions - Change your Mindset, Public Speaking. **Unit 2.LeadershipDevelopment:** Case Studies– APJ Abdul Kalam, DeepaMalik, Maharana Pratap, N Narayan Murthy etc. **Unit 3. Disaster management:** Disaster Management Capsule, Organization, Types of Disasters, Essential Services, Assistance, Civil Defense Organization. **Unit 4.Adventure:**AdventureActivities **Unit 5. Border & Coastal Areas:** History, Geography &Topography of Border/ Coastal Areas. **Unit 6. Drill:** Arm Drill, Rifle ke saath Savdhan, Vishram aur Aram se, Rifle ke saath Parade Paraur Saj, Riflekesaath Visarjan, LineTod, Bhumi Shastra aur Uthao Shastra, BagalShastra aur Baju Shastra. **Unit 7.WeaponTraining**: Short Range firing. **Unit 8.MapReading:**SettingofMap,FindingsNorthandOwnPosition **Unit 9.Field Craft & Battle Craft:** Observation, Camouflage, Concealment. **Unit 10. Obstacle Training:** Obstacle training - Introduction, Safety-measures, Benefits. Obstacle Course- Straight balance, Clear Jump, Gate Vault, Zig- Zag Balance, High Wall	50

SEMESTER-V & VI					
PHYSICAL EDUCATION(PE) **Category: NCMC**					
Course Code	:	B24NCK593/693	CIE	:	100 Marks
Teaching Hours L : T : P	:	1:0:0	SEE	:	--
Total Hours	:	--	Total	:	100 Marks
Credits	:	--	SEE Duration	:	--

Semester	Course
III	Fitness Components Kabaddi / KhoKho
IV	Athletics Volleyball Throw ball
V	Athletics Football / Hockey
V	Athletics Cricket / Base ball
VI	Athletics Netball / Basketball
VI	Individual Games Handball / Badminton

Notes:

- One Hour of Lecture is equal to 1 Credit
- One Hour of Tutorial is equal to1 Credit (Except Languages)
- Two Hours of Practical is equal to 1 Credit
- SEE: Semester End Examination
- CIE: Continuous Internal Examination
- L+T+P: Lecture + Tutorial + Practical

Guideline for Athletic and Sports

Semester & Course Code	Course Title	Content	No. of Hours
3rd Semester B24NCK393	**Fitness Components**	Meaning and Importance, Fit India Movement, Definition of fitness, Components of fitness, Benefits of fitness, Types of fitness and Fitness tips. ***Practical Components: Speed, Strength, Endurance, Flexibility, and Agility*** **KABADDI** **A. Fundamental skills** ➢ Skills in Raiding: Touching with hands, Use of leg-toe touch, squat leg thrust, side kick, mule kick, arrow fly kick, crossing of baulk line. Crossing of Bonus line. ➢ Skills of holding the raider: Various formations, catching from particular position, different catches, catching formation and techniques. ➢ Additional skills in raiding: Escaping from various holds, techniques of escaping from chain formation, offense and defense. ➢ Game practice with application of Rules and Regulations. **B. Rules and their interpretations and duties of the officials.**	Total-32 hours 2 hours / week
	Speed Strength Endurance Agility Flexibility		
	Kho kho	**A. Fundamental skills** ➢ Skills in Chasing: Sit on the box (Parallel & Bullet toe method), Get up from the box (Proximal & Distal foot method), Give Kho (Simple, Early, Late & Judgment), Pole Turn, Pole Dive, Tapping, Hammering, Rectification of foul. ➢ Skills in running: Chain Play, Ring play and Chain & Ring mixed play. ➢ Game practice with application of Rules and Regulations. **B. Rules and their interpretations and duties of the officials.**	
	Kabaddi	**A. Fundamental skills** 1. Skills in Raiding: Touching with hands, Use of leg-toe touch, squat leg thrust, side kick, mule kick, arrow fly kick, crossing of baulk line. Crossing of Bonus line. 2. Skills of holding the raider: Various formations, catching from particular position, different catches, catching formation and techniques. 3. Additional skills in raiding: Escaping from various holds, techniques of escaping from chain formation, offense and defense. 4. Game practice with application of Rules and Regulations. **B. Rules and their interpretations and duties of the officials**	

4th Semester **B24NCK493**	**Athletics** **Track-**Sprints **Jumps-**Long Jump **Throws-**Shot Put	**Track Events** ➢ Starting Techniques: Standing start and Crouch start (its variations) use of Starting Block. ➢ Acceleration with proper running techniques. ➢ Finishing technique: Run Through, Forward Lunging and Shoulder Shrug. **Long Jump**: Approach Run, Take-off, Flight in the air (Hang Style / Hitch Kick) and Landing **Shot put:** Holding the Shot, Placement, Initial Stance, Glide, Delivery Stance and Recovery (Perry O'Brien Technique)	Total-32 hours 2 hours / week
	Volleyball	**A. Fundamental skills** Service: Under arm service, Side arm service, Tennis service, Floating service. Pass: Under arm pass, Over head pass. Spiking and Blocking. Game practice with application of Rules and Regulations **B. Rules and their interpretation and duties of officials.**	
	Throw ball	**A. Fundamental skills** Overhand service, Side arm service, two hand catching, one hand overhead return, side arm return. **B. Rules and their interpretations and duties of officials**	

5th Semester **B24NCK593**	**<u>Athletics</u>** **Track-11**0&400 Meters Hurdles **Jumps-**High Jump **Throws-**Discuss Throw	**110 Meters and 400 Meters:** Hurdling Technique: Lead leg Technique, Trail leg Technique, Side Hurdling, Over the Hurdles Crouch start (its variations) use of Starting Block. Approach to First Hurdles, In Between Hurdles, Last Hurdles to Finishing. **High jump**: Approach Run, Take-off, Bar Clearance (Straddle) and Landing. **Discus Throw**: Holding the Discus, Initial Stance Primary Swing, Turn, Release and Recovery (Rotation in the circle).	

5th Semester **B24NCK593**	Football	**A. Fundamental Skills** ➢ Kicking: Kicking the ball with inside of the foot, Kicking the ball with Full Instep of the foot, Kicking the ball with Inner Instep of the foot, Kicking the ball with Outer Instep of the foot and Lofted Kick. ➢ Trapping: Trapping-the Rolling ball, and the Bouncing ball with sole of the foot. ➢ Dribbling: Dribbling the ball with Instep of the foot, Dribbling the ball with Inner and Outer Instep of the foot. ➢ Heading: In standing, running and jumping condition. ➢ Throw-in: Standing throw-in and Running throw-in. ➢ Feinting: With the lower limb and upper part of the body. ➢ Tackling: Simple Tackling, Slide Tackling. ➢ Goal Keeping: Collection of Ball, Ballclearance-kicking, throwing and deflecting. ➢ Game practice with application of Rules and Regulations. **B. Rules and their interpretation and duties of officials.**	Total-32 hours 2 hours / week
	Hockey	**A. Fundamental Skills** ➢ Passing: Short pass, Long pass, push pass, hit ➢ Trapping. ➢ Dribbling and Dozing. ➢ Penalty stroke practice. ➢ Penalty corner practice. ➢ Tackling: Simple Tackling, Slide Tackling. ➢ Goal Keeping, Ball clearance-kicking, and deflecting. ➢ Game practice with application of Rules and Regulations. **B. Rules and their interpretation and duties of officials.**	
	Athletics **Track**-Relays **Jumps**-Triple Jump **Throws**-Javelin Throw	**Relay Race**: Starting, Baton Holding / Carrying, Baton Exchange in between zone, and Finishing. **Triple Jump**: Approach Run, Take-off, Flight in the Hop, Step, Jump and Landing. **Javelin Throw**: Grip, Carry, and Recovery (3/5 Impulse stride). Release.	Total-32 hours 2 hours / week
	CRICKET	**A. Fundamental Skills** ➢ Batting-Forward Defense Stroke, Backward Defense Stroke, Off Drive, On Drive, Straight Drive, Cover Drive, Square Cut. ➢ Bowling-Out-swing, In-swing, Off Break, Leg Break and Googly. ➢ Fielding: Catching - The High Catch, The Skim Catch, The Close Catch and throwing at the stumps from different angles. Long Barrier and Throw, Short Throw, Long Throw, Throwing on the Turn. ➢ Wicket Keeping **B. Rules and their interpretation and duties of officials.**	

	BASEBALL	**A. Fundamental Skills** Player Stances–walking, extending walking, L stance, cat stance. Grip – standard grip, choke grip. Batting – swing and bunt. Pitching. Baseball: Slider, fast pitch, curve ball, drop ball, rise ball, change up, knuckle ball, screw ball. **B. Rules and their interpretation and duties of officials.**	

6th Semester **B24NCK693**	**Athletics** Combined Events-Heptathlon & Decathlon **Jumps**- Pole Vault **Throws**-Hammer Throw	Combined Events: Heptathlon all the7 events Decathlon: All10Events **Pole Vault**: Approach Run, Planting the Pole, Take-off, Bar Clearance and Landing. **Hammer Throw**: Holding the Hammer, Initial Stance Primary Swing, Turn, Release and Recovery (Rotation in the circle).	Total-32 hours 2 hours / week
	Basketball	**A. Fundamental Skills** ➢ Passing: Two hands Chest Pass, Two hands Bounce Pass, One hand Base ball Pass, Side arm Pass, Overhead Pass, Hook Pass. ➢ Receiving: Two hand receiving, one hand receiving, Receiving in stationary position, receiving while jumping and Receiving while Running. ➢ Dribbling: How to start dribble, drop dribble, High Dribble, Low Dribble, Reverse Dribble, Rolling Dribble. ➢ Shooting: Lay-up shot and its variations, one hand set shot, two hands jump shot, Hook shot, Free Throw. ➢ Rebounding: Defensive rebound and Offensive rebound. ➢ Individual Defence: Guarding the player with the ball and without the ball, pivoting. ➢ Game practice with application of Rules and Regulations. **B. Rules and their interpretation and duties of officials.**	
	Netball	**A. Fundamental skills** ➢ Catching: one handed, two handed, with feet grounded and in flight. ➢ Throwing (Different passes and their uses): One hand passes (shoulder, high shoulder, underarm, bounce, lob), two hand passes (Push, overhead and bounce). ➢ Footwork: Landing on one foot, landing on two feet, Pivot, Running pass. ➢ Shooting: One hand, forward step shot, and back ward step shot.	

		➢ Techniques of free dodge and sprint, sudden sprint, sprint and stop, sprinting with change at speed. ➢ Defending: Marking the player, marking the ball, blocking, inside the circle, outside the circle. Defending the circle edge against the passing. ➢ Intercepting: Pass and shot. ➢ Game practice with application of Rules and Regulations. **B. Rules and their interpretation and duties of officials.**	
	Individual games Shuttle Badminton	**A. Fundamental skills** ➢ Basic Knowledge: Various parts of the Racket and Grip. ➢ Service: Short service, Long service, Long-high service. ➢ Shots: Over head shot, Defensive clear shot, Attacking clear shot, Drop shot, Net shot, Smash. ➢ Game practice with application of Rules and Regulations. **B. Rules and their interpretation and duties of officials.**	Total-32 hours 2 hours / week
	Table Tennis	**A. Fundamental skills** ➢ Basic Knowledge: Various parts of the Racket and Grip (Shake Hand & Pen Hold Grip). ➢ Stance: Alternate & Parallel. ➢ Push and Service: Backhand & Forehand. ➢ Chop: Backhand & Forehand. ➢ Receive: Push and Chop with both Backhand & Forehand. ➢ Game practice with application of Rules and Regulations. **B. Rules and their interpretation and duties of officials.**	
	Hand ball	**A. Fundamental skills** ➢ Catching, Throwing and Ball control, ➢ Goal Throws: Jump shot, Center shot, Dive shot, Reverse shot. ➢ Dribbling: High and low. ➢ Attack and counter attack, simple counter attack, counter attack from two wings and center. ➢ Blocking, Goal Keeping and Defensive skills. ➢ Game practice with application of Rules and Regulations. **B. Rules and their interpretation and duties of officials.**	
	Ball Badminton	**A. Fundamental skills** ➢ Basic Knowledge: Various parts of the Racket and Grip. ➢ Service: Short service, Long service, Long-high service. ➢ Shots: Over head shot, Defensive clear shot, Attacking clear shot, Drop shot, Net shot, Smash. ➢ Game practice with application of Rules and Regulations. **B. Rules and their interpretation and duties of officials.**	

REFERENCES

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2. Bandopadhyay, K. Sarir Siksha Parichay, Classic Publishers, Kolkata.
3. Petipus, et al. Athlete's Guide to Career Planning, Human Kinetics.
4. Dharma, P. N. Fundamentals of Track and Field, Khel Sahitya Kendra, New Delhi.
5. Jain, R. Play and Learn Cricket, Khel Sahitya Kendra, New Delhi.
6. Vivek Thani, Coaching Cricket, Khel Sahitya Kendra, New Delhi.
7. Saha, A. K. Sarir Siksher Ritiniti, Rana Publishing House, Kalyani.
8. Bandopadhyay, K. Sarir Siksha Parichay, Classic Publishers, Kolkata
9. Naveen Jain, Play and Learn Basketball, Khel Sahitya Kendra, New Delhi.
10. Dubey, H. C. Basketball, Discovery Publishing House, New Delhi.
11. Rachana Jain, Teach Yourself Basketball, Sports Publication.
12. Jack Nagle, Power Pattern Of fences for winning basketball, Parker Publishing Co., New York. 13 Renu Jain, Play and Learn Basketball, Khel Sahitya Kendra, New Delhi.
13. Sally Kus, Coaching Volleyball Successfully, Human Kinetics.
14. Saha, A. K. Sarir Siksher Ritiniti, Rana Publishing House, Kalyani.
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SEMESTER-V & VI					
YOGA **Category: NCMC**					
Course Code	:	B24NCK594/694	CIE	:	100 Marks
Teaching Hours L : T : P	:	1:0:0	SEE	:	--
Total Hours	:	--	Total	:	100 Marks
Credits	:	--	SEE Duration	:	--

Semester	Course
III Semester	1) Introduction of Yoga, Aim and Objectives of yoga, Prayer 2) Brief introduction of yogic practices for common man 3) Rules and regulations 4) Misconceptions of yoga 5) Suryanamaskara 6) Different types of Asanas a. Sitting b. Standing c. Prone line d. Supine line
IV Semester	1) Patanjali's Ashtanga Yoga 2) Suryanamaskara 3) Different types of Asanas a. Sitting b. Standing c. Prone line d. Supine line 4) Kapalbhati 5) Pranayama
V Semester	1) Patanjali's Ashtanga Yoga 2) Surya namaskara 3) Different types of Asanas a. Sitting b. Standing c. Proneline d. Supineline 4) Kapalbhati 5) Pranayama

	1) Patanjali's Ashtanga Yoga 2) Suryanamaskara 3) Different types of Asanas a. Sitting b. Standing c. Prone line d. Supine line 4) Kapalbhati 5) Pranayama
VI Semester	1) Patanjali's Ashtanga Yoga 2) Suryanamaskara 3) Different types of Asanas a. Sitting b. Standing c. Prone line d. Supine line 4) Kapalbhati 5) Pranayama
	1) Patanjali's AshtangaYoga 2) Suryanamaskara 3) Different types of Asanas a. Sitting b. Standing c. Prone line d. Supine line 4) Kapalbhati 5) Pranayama 6) Shat Kriyas

Notes:

- One Hour of Lectureisequalto1Credit
- One Hour of Tutorial is equal to 1Credit (Except Languages)
- Two Hours of Practical is equal to 1Credit
- SEE: Semester End Examination
- CIE: Continuous Internal Examination
- L+T+P: Lecture + Tutorial + Practical

Guidelines for Yoga Syllabus

Semester & Course Code	Course Title	Content	No. of Hours
3rd Semester B24NCK394	Introduction of Yoga, Aim and Objectives of yoga, Prayer	Yoga, its origin, history and development. Yoga, its meaning, definitions. Different schools of yoga, importance of prayer	Total-32 hours 2 hours / week
	Brief introduction of yogic practices for common man	Yogic practices for common man to promote positive health	
	Rules and regulations	Rules to be followed during yogic practices by practitioner	
	Misconceptions of yoga	Yoga its misconceptions, Difference between yogic and non yogic practices.	
	Suryanamaskara	Suryanamaskar prayer and its meaning, Need, importance and benefits of Suryanamaskar12 count, 2 rounds	
	Different types of Asanas Sitting ➢ Padmasana ➢ Vajrasana Standing ➢ Vrikshana ➢ Trikonasana Prone line ➢ Bhujangasana ➢ Shalabhasana Supine line ➢ Utthitadvipadasana ➢ Ardhahalasana	Asana, Need, importance of Asana. Different types of asana. Asana its meaning by name, technique, precautionary measures and benefits of each asana.	

4th Semester **B24NCK494**	Patanjali's Ashtanga Yoga ➢ Yama ➢ Niyama	Patanjali's Ashtanga Yoga its need and importance. <u>Yama:</u> Ahimsa, satya, asteya, brahmacarya, aparigraha. <u>Niyama:</u> shoucha, santosh, tapa, svaadhyaya, Eshvara pranidhan	Total-32 hours 2 hours / week
	Suryanamaskara	Suryanamaskar 12 count, 4 rounds	
	Different types of Asanas Sitting ➢ Sukhasana ➢ Paschimottanasana Standing ➢ Ardhakati Chakrasana ➢ Parshva Chakrasana Prone line ➢ Dhanurasana Supine line ➢ Halasana ➢ Karna Peedasana	Asana, Need, importance of Asana. Different types of asana. Asana its meaning by name, technique, precautionary measures and benefits of each asana.	
	Kapalabhati	Meaning, importance and benefits of Kapalabhati. 40 strokes/min, 3 rounds	
	Pranayama ➢ Suryanuloma–Viloma ➢ Chandranuloma-Viloma ➢ Suryabhedana ➢ ChandraBhedana ➢ Nadishodhana	Meaning, Need, importance of Pranayama. Different types. Meaning by name, technique, precautionary measures and benefits of each Pranayama	

5th Semester **B24NCK594**	Ashtanga Yoga ➢ Asana ➢ Pranayama	Patanjali's Ashtanga Yoga its need and importance.	Total-32 hours 2 hours / week
	Suryanamaskara	Suryanamaskar 12 count, 6 rounds	
	Different types of Asanas Sitting ➢ Ardha Ushtrasana ➢ Vakrasana Standing ➢ Urdhva Hastothanasana ➢ Hastapadasana Prone line ➢ Padangushtha Dhanurasana Supine line ➢ Sarvangasana ➢ Chakraasana	Asana, Need, importance of Asana. Different types. Asana its meaning by name, technique, precautionary measures and benefits of each asana.	
	Kapalabhati	Revision of practice 50 strokes/min, 3 rounds	
	Pranayama ➢ Surya Bhedana ➢ Ujjayi	Meaning, Need, importance of Pranayama. Different types. Meaning by name, technique, Precautionary measures and benefits of each Pranayama.	
	Ashtanga Yoga ➢ Pratyahara ➢ Dharana	Patanjali's Ashtanga Yoga its need and importance.	Total-32 hours 2 hours / week
	Suryanamaskara	Revisionofpractice12count, 8 rounds	
	Different types of Asanas Sitting ➢ AakarnaDhanurasana ➢ YogamudrainPadmasana Standing ➢ ParivrittaTrikonasana ➢ Utkatasana Prone line ➢ PoornaBhujangasana/	Asana, Need, importance of Asana. Different types, Asana by name, technique, precautionary measures and benefits of each asana.	

	Rajakapotasana Supine line ➢ Navasana/Noukasana ➢ Pavanamuktasana		
	Kapalabhati	Revision of practice 60 strokes/min, 3 rounds	
	Pranayama ➢ Sheetali ➢ Sheektari	Meaning, Need, importance of Pranayama. Different types. Meaning by name, technique, precautionary measures and benefits of each Pranayama	

6th Semester **B24NCK694**	Ashtanga Yoga ➢ Dhyana (Meditation) ➢ Samadhi	Patanjali's Ashtanga Yoga its need and importance.	Total-32 hours 2 hours / week
	Suryanamaskara	Revision of practice 12count, 10rounds.	
	Different types of Asanas Sitting ➢ Vibhakta Paschimottanasana ➢ Yogamudra inVajrasana Standing ➢ Parshvakonasana ➢ Ekapadbaddhapadmottanasana Prone line balancing ➢ Mayurasana Supine line ➢ Sarvangasana ➢ Setubandhasana ➢ Shavasanaa (Relaxation poisture)	Asana, Need, Importance of Asana. Different types, Asana by name, technique, precautionary measures and benefits of each asana.	
	Kapalabhati	Revision of practice 80 strokes/min, 3 rounds	

	Pranayama ➢ Bhastrika ➢ Bhramari	Meaning, Need, importance of Pranayama. Different types. Meaning by name, technique, Precautionary measures and benefits of each Pranayama.	
	Suryanamaskara	Revision of practice 12count, 12 rounds.	Total-32 hours 2 hours / week
	Different types of Asanas Sitting ➢ Bakasana ➢ Hanumanasana ➢ Ekapada Rajakapotasana Standing ➢ Vatayanasana ➢ Garudasana ➢ Natarajasana Balancing ➢ Sheershasana Supine line ➢ 1.Setubandha Sarvangasana ➢ Shavasanaa (Relaxation poisture)	Asana, Need, importance of Asana. Different types, Asana by name, technique, precautionary measures and benefits of each asana.	
	Kapalabhati	Revision of practice 100 strokes/min, 3 rounds.	
	Pranayama ➢ Nadishodhana ➢ Ujjai ➢ Bhramari	Revision of practices	
	ShatKriyas ➢ Jalaneti & sutraneti ➢ Nouli (only for men) ➢ Sheetkarma Kapalabhati	Meaning, Need, importance of Shatkriya. Different types. Meaning by name, technique, precautionary measures and benefits of each Kriya	

Book for Reference:

- Swami Kuvulyananda: Asma (Kavalyadhama, Lonavala)
- Tiwari, O P: Asana Why and How

- Ajitkumar: Yoga Pravesha (Kannada)
- Swami Satyananda Saraswati: Asana Pranayama, Mudra, Bandha (Bihar School of yoga, Munger)
- Swami Satyananda Saraswati: Surya Namaskar (BiharSchoolofyoga,Munger)
- Nagendra H R: The art and science of Pranayama
- Tiruka: Shatkriyegalu (Kannada)
- Iyengar B K S: Yoga Pradipika (Kannada)
- Iyengar B K S: Light on Yoga (English)

SEMESTER-V & VI					
MUSIC **Category: NCMC**					
Course Code	:	B24NCK595/695	CIE	:	100 Marks
Teaching Hours L : T : P	:	1:0:0	SEE	:	--
Total Hours	:	--	Total	:	100 Marks
Credits	:	--	SEE Duration	:	--

Course Objectives	
1.	Identify the major traditions of Indian music, both through notations and aurally.
2.	Analyze the compositions with respect to musical and lyrical content
3.	Demonstrate an ability to use music technology appropriately in a variety of setting.

Module – 1	**No. of Hours**
Preamble: Contents of the curriculum intend to promote music as language to develop an analytical, Creative, and intuitive Understanding. For this the student must experience music through study and direct participation in improvisation and composition. Origin of the Indian Music: Evolution of the Indian music system, Understanding of Shruthi, Nada, Swara, Laya, Raga Tala, Mela.	3
Module – 2	**No. of Hours**
Compositions: Introduction to the types of composition in Carnatic Music- Geethe, Jath i, Swara, Swarajathi, Varna, Krithi, and Thillana, Notation System.	3
Module – 3	**No. of Hours**
Composers: Biography and contributions of Purandaradasa, Thyagaraja, Mysoro Vasudevacharya.	3
Module – 4	**No. of Hours**
Music Instruments: Classification and construction of string instruments, wind instrurments, percussion instruments, Idiophones (Ghana Vaadya), Examples of each class of Instrum ents	3
Module – 5	**No. of Hours**
Abhyasa Gana: Singing the swara exercises (Sarale Varase Only), Botation writing for Sarale Varase and Suladi Saptha Tala (Only in Mayamalavagowla Raga), Singing 4 Geethe in M alahari, and one jathi Swara, One Krithi in a Mela raga	14

Course Outcomes: At the end of the course, the students will be able to	
CO1	Discuss the Indian system of music and relate it to other genres (Cognitive DOmain)
CO2	Experience the emotions of composer and develop empathy (Affective Domain)
CO3	Respond to queries on various patterns in a composition (Psycho Motor Domain)

Text Books	
1.	Vidushi Vasantha Madhavi, "Theory of Music", Prism Publication, 2007.
2.	T Sachidevi and T Sharadha (Thirumalai Sisters), Karnataka Sangeetha Dharpana- Vol. 1 (English), Shreenivaas Prakaashana, 2018.

Reference Text Books	
1.	Lakshminarayana Subramaniam, Viji Subramanaim, "Classical Music of India: A Practical Guige", Tranqueber 2018.
2.	R. Rangaramanuja Ayyangar, "History of South Indian (Carnatic) Music", Vipanci Charitable Trust; Third edition, 2019.
3.	Ethel Rosenthal, "The Story of Indian Music and Its Istruments: A Study of the Present and a Record of the Past", Pilgrims Publishing, 2007.
4.	Carnatic Music, National Institute of Open Schooling, 2019.