MOOGAMBIGAI CHARITABLE AND EDUCATIONAL TRUST

Rajarajeswari College of Engineering

(An Autonomous Institution under Visvesvaraya Technological University, Belagavi)
#14, Ramohalli Cross, Kumbalagodu, Mysore Road, Bengaluru–560074

Electronics and Communication Engineering

Bachelor of Engineering (B.E)

Scheme and Syllabus of III & IV Semester

(2024 Scheme)

VISION

To empower young minds through technology, research and innovation, to produce technically competent and socially responsible professionals in higher education.

MISSION

1. To deliver excellence in education through innovative teaching, impactful research, and continuous skill development, preparing students to meet global challenges with technical expertise and ethical responsibility.
2. To foster a transformative learning environment that integrates technology, research and practical experience, empowering students to become skilled professionals and socially conscious leaders.
3. To cultivate a culture of lifelong learning and professional excellence by encouraging creativity, research, and community engagement, equipping students with the skills to thrive in a dynamic world.
4. To provide a holistic educational experience that combines advanced technology, hands-on research, and community-focused learning, shaping students into competent, ethical professionals who contribute positively to society.

QUALITY POLICY

Rajarajeswari College of Engineering is committed to imparting quality technical education that nurtures competent, ethical professionals with global relevance. We ensure academic excellence through a dynamic, outcome-based curriculum, experienced faculty, and cutting-edge infrastructure. Continuous improvement is driven by innovation, research and strong industry collaboration. We foster holistic development and a progressive environment that supports lifelong learning, teamwork, and professional growth.

CORE VALUES

Academic Excellence, Integrity, Innovation, Global Competence, Continuous Improvement.

Electronics and Communication Engineering

DEPARTMENT VISION

Actualize high Quality Electronics and Communication Engineering professionals showcasing Innovation, Research and Performance in the Frontier areas and capable of working local, global, environment contributing for Societal development through sustainable technology keeping high moral values.

DEPARTMENT MISSION

1. To give strong fundamental and contemporary knowledge to students with excellent curriculum and faculty.
2. Promoting Innovation and Research by creating ambiance by collaborating Industry & academics also involving them to do societal beneficial projects.
3. Imparting ethics to students through relevant practices.

PROGRAM OUTCOMES (POs)

PO1: Engineering Knowledge: Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization as specified in WK1 to WK4 respectively to develop to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development. (WK1 to WK4)

PO3: Design/Development of Solutions: Design creative solutions for complex engineering problems and design/develop systems /components / processes to meet identified needs with consideration for the public health and safety, whole-life cost, net zero carbon, culture, society and environment as required. (WK5)

PO4: Conduct Investigations of Complex Problems: Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modeling, analysis & interpretation of data to provide valid conclusions. (WK8).

PO5: Engineering Tool Usage: Create, select and apply appropriate techniques, resources and modern engineering & IT tools, including prediction and modeling recognizing their limitations to solve complex engineering problems. (WK2 and WK6)

PO6: The Engineer and The World: Analyze and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health, safety, legal framework, culture and environment. (WK1, WK5, WK7).

PO7: Ethics: Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national & international laws. (WK9)

PO8: Individual and Collaborative Team work: Function effectively as an individual, and as a member or leader in diverse/multi-disciplinary teams.

PO9: Communication: Communicate effectively and inclusively within the community and society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations considering cultural, language, and learning differences

PO10: Project Management and Finance: Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.

PO11: Life-Long Learning: Recognize the need for, and have the preparation and ability for i) independent and life-long learning ii) adaptability to new and emerging technologies and iii) critical thinking in the broadest context of technological change. (WK8)

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: Able to take up career in the Electronics & Communication industries to contribute by innovative design and products to help society.

PEO2: Capable to work in team with good communication skills, leadership qualities and ethics.

PEO3: Professional empowering by taking up higher education or updating knowledge in line with the changing trends of technology.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Demonstrate the competency to analyze the real time problems related to Electronics and communication industry and able to design and develop products with the cutting edge technology.

PSO2: Demonstrate leadership qualities to resolve the complex multidisciplinary engineering, societal challenges in the ethical manner.

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Department of Electronics and Communication Engineering

Scheme of Teaching and Examinations: 2024

(Effective from the Academic Year 2025-26)

Semester: III

S.No	Course Category and Course Code		Course Title	TD / PSB	Teaching Hours / Week & Credits					Examination			
					Lecture	Tutorial	Practical	SDA	Credits	CIE Marks	SEE Duration Hrs	SEE Marks	Total Marks
					L	T	P	S					
1.	BSC	B24ME301	Mathematics- III for EE (Common to ECE, EEE)	Maths	3	0	0	0	3	50	3	50	100
2.	PCC	B24EC302	Network Analysis	ECE	3	0	0	0	3	50	3	50	100
3.	IPCC	B24EC303	Linear Integrated Circuits and Applications	ECE	3	0	2	0	4	50	3	50	100
4.	IPCC	B24EC304	Digital System Design using Verilog	ECE	3	0	2	0	4	50	3	50	100
5.	PCCL	B24EC305L	Analog and Digital Electronics Lab	ECE	0	0	2	0	1	50	3	50	100
6.	ESC	B24YY36X	ESC/ETC/PLC - III	ECE	3	0	0	0	3	50	3	50	100
7.	UHV	B24SEC307	Social Connect and Responsibility	Any Dept.	0	0	2	0	1	50	3	50	100
8.	AEC/ SEC	B24YY38X	Ability Enhancement Course / Skill Enhancement Course – III (Theory/Lab)	ECE	1 0	0 0	0 2	0	1	50	1 3	50	100
9.	NCMC	B24NCK39X	National Service Scheme / National Cadet Corps / Physical Education / Yoga /Music	HSMC	1	0	0		PP	50	-	-	50
								TOTAL	20	450		400	850

BSC: Basic Science Course, HSMC: Humanity Social sciences including Management courses, IPCC: Integrated Professional Core Course, PCC: Professional Core Course, PCCL: Professional Core Course laboratory, UHV: Universal Human Value Course, NCMC: Non-Credit Mandatory Course, AEC: Ability Enhancement Course, SEC: Skill Enhancement Course, ESC: Engineering Science Course, ETC: Emerging Technology Course, PLC: Programming Language Course L: Lecture, T: Tutorial, P: Practical S:SDA-Skill Development Activity, CIE: Continuous Internal Evaluation, SEE: Semester End Evaluation, PP/NP: Pass / Not Pass, YY: Programme Code (EC, CS, IS etc), X: 1/2/3/4, K: Indicates Common Course to all the streams of Engineering.

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Engineering Science Course /Emerging Technology Course / Programming Language Course (ESC/ETC/PLC) - III			
B24EC361	Power Electronics	B24EC362	Solid State Devices
B24EC363	Computer Organization and Architecture	B24EC364	OOPS with C++

Ability Enhancement Course / Skill Enhancement Course (AEC/SEC) – III			
B24EC381	C++ Programming Lab	B24EC382	IoT for Smart Infrastructure
B24EC383	Lab View Programming	B24EC384	Data structures using C

Non Credit Mandatory Courses (NCMC)			
B24NCK391	National Service Scheme (NSS)	B24NCK392	National Cadet Corps (NCC)
B24NCK393	Physical Education (PE)	B24NCK394	Yoga
B24NCK395	Music		

All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE), National Cadet Corps (NCC), Music and Yoga (YOG) with the concerned coordinator of the course during the first week of III/IV/V/VI semesters. Colleges are required to submit the Continuous Internal Evaluation (CIE) marks for the activities completed by students under selected course each semester. The students should be allowed to engage in different activities/courses each semester. For example, a student who participates in sports in the 3rd semester could choose to undertake NSS in the next semester and Yoga in another semester. This approach aligns with the student-centric focus of the National Education Policy (NEP) 2022 and helps distribute the workload related Physical Education/NSS/Yoga/NCC/Music of more evenly across different departments. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities.

These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the course is mandatory for the award of degree.

HOD **Dean-Academics** **Principal**

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Department of Electronics and Communication Engineering

Scheme of Teaching and Examinations: 2024

(Effective from the Academic Year 2025-26)

Semester: IV

S. No	Course Category and Course Code		Course Title	TD / PSB	Teaching Hours / Week & Credits					Examination			
					Lecture	Tutorial	Practical	SDA	Credits	CIE Marks	SEE Duration Hrs	SEE Marks	Total Marks
					L	T	P	S					
1.	PCC	B24ME401	Mathematics - IV	Maths	3	0	0	0	3	50	3	50	100
2.	PCC	B24EC402	Electromagnetic Field Theory	ECE	3	0	0	0	3	50	3	50	100
3.	IPCC	B24EC403	Communication System - 1	ECE	3	0	2	0	4	50	3	50	100
4.	IPCC	B24EC404	Control Engineering	ECE	3	0	2	0	4	50	3	50	100
5.	PCCL	B24EC405L	Communication Systems Lab-1	ECE	0	0	2	0	1	50	3	50	100
6.	ESC	B24YY 46X	ESC/ETC/PLC - IV	ECE	3	0	0	0	3	50	3	50	100
7.	UHV	B24UHK407	Universal Human values	Any Dept.	1	0	0	0	1	50	1	50	100
8.	AEC/SEC	B24YY48X	Ability Enhancement Course / Skill Enhancement Course – III (Theory/Lab)	ECE	1 0	0 0	0 2	0	1	50	1 3	50	100
9.	NCMC	B24NCK49X	National Service Scheme / National Cadet Corps / Physical Education / Yoga/Music	HSMC	1	0	0		PP	50		-	50
								TOTAL	20	450		400	850

BSC: Basic Science Course, HSMC: Humanity Social sciences including Management courses, IPCC: Integrated Professional Core Course, PCC: Professional Core Course, PCCL: Professional Core Course laboratory, UHV: Universal Human Value Course, NCMC: Non-Credit Mandatory Course, AEC: Ability Enhancement Course, SEC: Skill Enhancement Course, ESC: Engineering Science Course, ETC: Emerging Technology Course, PLC: Programming Language Course L: Lecture, T: Tutorial, P: Practical S:SDA-Skill Development Activity, CIE: Continuous Internal Evaluation, SEE: Semester End Evaluation, PP/NP: Pass / Not Pass, YY: Programme Code (EC, CS, IS etc), X: 1/2/3/4, K: Indicates Common Course to all the streams of Engineering.

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Engineering Science Course /Emerging Technology Course / Programming language Course (ESC/ETC/PLC) - IV			
B24EC 461	Microcontrollers	B24EC 462	Embedded Systems and IOT Design
B24EC 463	Smart Sensors	B24EC 464	JAVA Programming (Common to ECE,EEE)

Ability Enhancement Course / Skill Enhancement Course (AEC/SEC) – IV			
B24EC481	Programmable Logic Controllers	B24EC482	Introduction to Artificial Intelligence
B24EC483	Microcontrollers Lab	B24EE484	Arduino and Raspberry Pi lab (Common to ECE, EEE)

Non Credit Mandatory Courses (NCMC)			
B24NCK491	National Service Scheme (NSS)	B24NCK492	National Cadet Corps (NCC)
B24NCK493	Physical Education (PE)	B24NCK494	Yoga
B24NCK495	Music		

All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE), National Cadet Corps (NCC), Music and Yoga (YOG) with the concerned coordinator of the course during the first week of III/IV/V/VI semesters. Colleges are required to submit the Continuous Internal Evaluation (CIE) marks for the activities completed by students under selected course each semester. The students should be allowed to engage in different activities/courses each semester. For example, a student who participates in sports in the 3rd semester could choose to undertake NSS in the next semester and Yoga in another semester. This approach aligns with the student-centric focus of the National Education Policy (NEP) 2022 and helps distribute the workload related Physical Education/NSS/Yoga/NCC/Music of more evenly across different departments. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities.

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HoD **Dean-Academics** **Principal**

III - Semester Syllabus

SEMESTER-III					
Mathematics-III for EE **Category: BSC** **(Common to EEE, ECE)**					
Course Code	:	B24ME301	CIE	:	50 Marks
Teaching Hours L : T : P	:	3:0:0	SEE	:	50 Marks
Total Hours	:	45(T)	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Objectives	
1.	Learn to use the Fourier series to represent periodical physical phenomena in engineering analysis and to enable the student to express periodic functions using the Fourier series.
2.	Analyze signals in terms of Fourier transforms and z transforms.
3.	Have an insight into solving ordinary differential equations by using Laplace transform techniques.
4.	To introduce the concept of random variables, probability distributions, specific discrete and continuous distributions with practical application in Engineering and social life situations.
5.	To understand the random process for use in communication &analyzing data in engineering.

Module-1:Fourier series	**No. of Hours**
Periodic functions, Dirichlet's condition. Fourier series expansion of functions with period $2\pi$and with arbitrary period: periodic rectangular wave, Half-wave rectifier, rectangular pulse, Saw tooth wave. Half-range Fourier series. Triangle and half range expansions, Practical harmonic analysis. **Self-study:** Typical waveforms, complex form of Fourier series **Applications:** Analyze and predict the behavior of circuits and systems, Vibration analysis.	9
Module-2:FourierTransforms and Z-transforms	**No. of Hours**
Infinite Fourier transforms Fourier cosine and sine transforms, Inverse Fourier transforms, Inverse Fourier cosine and sine transforms. Z-transform-definition, Standard Z-transforms, Damping and shifting rules, Problems. Initial value and final value theorems, Inverse Z-transform and applications to solve difference equations. **Self-study:** Convolution theorems of Fourier Transforms. **Applications:** Digital Signal Processing (DSP), Control Systems Engineering.	9
Module 3:Laplace Transforms	**No. of Hours**
Definition and Laplace transforms of elementary functions (statements only). Problems on Laplace's Transform of $e^{at}f(t)$, $t^n f(t)$, $\frac{f(t)}{t}$. Laplace transforms of Periodic functions (statement only) and unit-step function – problems. Inverse Laplace transforms definition and problems, Convolution theorem to find the inverse Laplace transforms (without Proof) problems. Laplace transforms of derivatives, solution of differential equations. **Self-study:** Solution of simultaneous first-order differential equations. **Applications:** Signals and systems, Control systems, LR, CR & LCR circuits.	9
Module-4: Probability Distributions	**No. of Hours**
Random variables-discrete and continuous Probability distribution function, cumulative distribution function, mean and variance, Binomial, Poisson, Exponential and Normal distribution (without proofs for mean and SD) – Problems. **Sampling Theory**: Introduction to sampling distributions, standard error, Type-I and Type-II errors. Student's t-distribution, Chi-square distribution as a test of goodness of fit. **Self-study:** Test of hypothesis for means, single proportions only. **Applications:** Quality control, Signal processing, Reliability analysis.	9
Module-5: Two dimensional Random variables	**No. of Hours**
Joint probability mass function, Marginal probability function, conditional probability function. Random Process: Classification of random process, description of random process, stationary random process – first order, second order and Strict-sense stationary processes, Autocorrelation and Cross-correlation functions. **Self-study:** covariance, correlation coefficient. **Application:** Bayesian network.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Demonstrate the Fourier series to study the behaviour of periodic functions and their applications in system communications, digital signal processing, and field theory.
CO2	To use Fourier transforms to analyze problems involving continuous-timesignals. To apply Z-Transform techniques to solve difference equations.
CO3	To understand the concept of Laplace transform and to solve initial value problems.
CO4	Apply discrete and continuous probability distributions in analyzing the probability models arising in the engineering field. Demonstrate the validity of testing the hypothesis.
CO5	To understand the random process for use in communication &analyzing data in engineering.

Text Books	
1.	B.S.Grewal:"Higher Engineering Mathematics", Khanna publishers,44th Edition.2018
2.	E.Kreyszig:"Advanced Engineering Mathematics", John Wiley & Sons,8th Edition.(Reprint),2016
3.	E.Kreyszig&V. Ramana: Advanced Engineering Mathematics",10th edition

Reference Text Books	
1.	V. Ramana: "Higher Engineering Mathematics", McGraw-Hill Education, 11th Edition.
2.	E.Kreyszig&V. Ramana: Advanced Engineering Mathematics",10th edition

Web links and Video lectures (e-Resources)

1. https://nptel.ac.in/courses/12286025
2. VTUEDUSATPROGRAMME –20
3. http://www.class-central.com/subject/math(MOOCs)

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
5. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50).

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and it carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO8	PO11
CO1	3	3	3	1	-	-	-	-	1	-	2
CO2	3	3	3	1	-	-	-	-	1	-	2
CO3	3	3	3	1	-	-	-	-	1	-	2
CO4	3	3	2	2	-	-	-	-	1	-	2
CO5	3	3	2	2	-	-	-	-	1	-	2

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-III					
NETWORK ANALYSIS **Category: PCC**					
Course Code	:	B24EC302	CIE	:	50 Marks
Teaching Hours L : T : P	:	3:0:0	SEE	:	50 Marks
Total Hours	:	45(T)	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Objectives	
1.	To understand the mesh and nodal techniques to solve an electrical network
2.	To Solve different problems related to electrical circuits using network theorems.
3.	To study the behavior of networks subjected to transient conditions.
4.	To Use applications of Laplace transform to solve network problems.
5.	To Study two port parameters for different electrical networks and RLC Series and parallel circuits.

Module – 1: Basic Concepts	**No. of Hours**
Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis with linearly dependent and independent sources for DC and AC networks.	9
Module – 2 : Network Theorems	**No. of Hours**
Superposition, Millman‘s theorems, Thevinin‘s and Norton‘s theorems, Maximum Power transfer theorem.	9
Module – 3: Transient behavior and initial conditions	**No. of Hours**
Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations	9
Module – 4: Laplace Transformation & Applications	**No. of Hours**
Solution of networks, step, ramp and impulse responses, waveform Synthesis.	9
Module – 5: Two port network parameters and Resonance	**No. of Hours**
Two port network parameters: Definition of Z, Y, h and Transmission parameters, modelling with these parameters, relationship between parameters sets. **Resonance:** Series Resonance: Variation of Current and Voltage with Frequency, Selectivity and Bandwidth, Q-Factor, Circuit Magnification Factor, Selectivity with Variable Capacitance, Selectivity with Variable Inductance. Parallel Resonance: Selectivity and Bandwidth, Maximum Impedance Conditions with C, L and f Variable, current in Anti-Resonant Circuit, The General Case-Resistance Present in both Branches.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Determine currents and voltages using source transformation/ source shifting/ mesh/ nodal analysis and reduce given network using star-delta transformation/source transformation/ source shifting
CO2	Solve network problems by applying Superposition/Thevenin‘s/ Norton‘s/ Maximum Power Transfer/ Millman‘s Network Theorems and electrical laws to reduce circuit complexities and to arrive at feasible solutions.
CO3	Calculate current and voltages for the given circuit under transient conditions.
CO4	Apply Laplace transform to solve the given network.
CO5	Solve the given network using specified two port network parameter like Z or Y or T or h and Understand the concept of resonance.

Text Books	
1.	M.E. Van Valkenberg (2000), ―Network analysis‖, Prentice Hall of India, 3rd edition, 2000, ISBN: 9780136110958
2.	Roy Choudhury, ―Networks and systems‖, 2nd edition, New Age International Publications, 2006, ISBN: 9788122427677

Reference Text Books	
1.	Hayt, Kemmerly and Durbin ―Engineering Circuit Analysis‖, TMH 7th Edition,2010
2.	J. David Irwin /R. Mark Nelms, ―Basic Engineering Circuit Analysis‖, John Wiley, 8th edition, 2006
3.	Charles K Alexander and Mathew N O Sadiku, ― Fundamentals of Electric Circuits‖, Tata McGraw-Hill, 3rd Edition, 2009.

Web links and Video lectures (e-Resources)
1. Network Analysis - Course (nptel.ac.in)
2. Network Theory Study Notes (Handwritten) Free PDF - GATE / FE / ESE (newtondesk.com)

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CO2	3	1	2	1	1	-	-	-	-	1	1
CO3	3	1	2	1	1	-	-	-	-	1	1
CO4	3	1	2	1	1	-	-	-	-	1	1
CO5	3	1	2	1	1	-	-	-	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-III					
LINEAR INTEGRATED CIRCUITS AND APPLICATIONS **Category: IPCC**					
Course Code	:	B24EC303	CIE	:	50 Marks
Teaching Hours L : T : P	:	3:0:2	SEE	:	50 Marks
Total Hours	:	45(T)+15(P)	Total	:	100 Marks
Credits	:	4	SEE Duration	:	3 Hrs

Course Objectives	
1.	To understand the basic principles of operational Amplifier.
2.	To study and design linear and non linear circuits.
3.	To study and design the active filters such as Butterworth low pass and high pass, Bandpass and Bandstop filters.
4.	To understand the principles of various ADC / DAC architectures.
5.	To understand the operation and applications of IC 555 timers, phase locked loop, voltage regulators.

Module – 1: Operational Amplifiers (op-amp)	**No. of Hours**
Block diagram representation of a typical op-amp, Operational amplifier parameters : input offset voltage, input offset current, input bias current, common mode rejection ratio, supply voltage rejection ratio, input and output resistance, gain bandwidth product. Ideal operational amplifier, equivalent circuit of op-amp, open loop op-amp configuration - differential amplifier, inverting amplifier, Non-inverting amplifier. Text1 : 1.3, 2.2, 2.3, 2.4, 2.6	8
Module – 2: Op-amp with Negative feedback and General Linear applications	**No. of Hours**
Block diagram representation of feedback configurations, Voltage series feedback amplifier, Voltage shunt feedback amplifier, differential amplifiers, General Linear applications – summing, scaling, averaging amplifiers, differential configuration – subtractor, Instrumentation amplifier, Integrator and differentiator. Text1 : 3.2, 3.3.1 – 3.3.5, 3.4.1 – 3.4.4, 3.5, 6.5.1 – 6.5.3b, 6.6, 6.6.1, 6.12, 6.13	9
Module – 3: Active filters and Oscillators	**No. of Hours**
Active filters, first order low pass Butterworth filter, second order low pass Butterworth filter, first order high pass Butterworth filter, second order high pass Butterworth filter, Bandpass filters, Band reject filters. Oscillators: Principles, Phase shift oscillator, Wein bridge oscillator. Text1 : 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 7.11.1, 7.12, 7.13	9
Module – 4: Op-Amp circuits	**No. of Hours**
Basic comparator, zero crossing detector, Schmitt trigger, Digital to Analog converters – Binary weighted resistors, with R and 2R resistors, Analog to digital converters – successive approximation type, small signal half wave rectifier, absolute value output circuit, peak detector, sample and hold circuit. Text1 : 8.2, 8.3, 8.4, 8.11.1a, 8.11.1.b, 8.11.2a, 8.12.2, 8.13, 8.14, 8.15	10
Module – 5: Specialized IC applications	**No. of Hours**
555 Timers, Monostable multi-vibrator, Monostable operation, Astable multi-vibrator, Astable operation, Phase locked loops – operating principles, phase detector, voltage controlled oscillator, voltage regulators – fixed voltage regulators, adjustable voltage regulator Text1: 9.4, 9.4.1a, 9.4.3, 9.4.3a, 9.5.1, 9.5.1a, c, 9.7.1, 9.7.2a	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Apply the basic concepts of operational Amplifier and its parameters.
CO2	Analyze the design of summing, averaging and instrumentation amplifier.
CO3	Apply the knowledge to design the op-amp active filters.
CO4	Analyze the design of op-amp comparators and data converter architectures.
CO5	Apply the knowledge to design the timing circuits and voltage regulators using linear ICs.

Text Books	
1.	Ramakanth A Gayakwad, Op-Amps and Linear Integrated Circuits, 4th Edition, Pearson Education, Prentice hall.

Reference Text Books	
1.	D Roy Choudhury, Shail B Jain, Linear Integrated circuits, 2nd Edition, New Age International Publishers.

Web links and Video lectures (e-Resources)
1. https://nptel.ac.in/courses/117107094
2. https://youtu.be/WFsPI8_ZKbc?si=LdD7SB4ZKKjVFcL1
3. https://youtu.be/ssEAzB8MR7g?si=EQ_naA2aXCD_GoiM

LABORATORY

Practical Component of IPCC (12 Experiments)

- Experiments using Pspice / MultiSIM
- Every experiment has to be designed, circuit to be drawn / constructed and executed in the specified software. Results are also to be noted and inferred.

Note: Standard design procedure to be adopted.

Sl. No	Name of the experiment
1.	To realize using op-amp a. Inverting Amplifier and Non-Inverting Amplifier b. Summing Amplifier and Difference amplifier
2.	To realize using op-amps an Instrumentation Amplifier.
3.	To realize using op-amps i) Differentiator ii)Integrator
4.	To realize using op-amps a Full wave Precision Rectifier.
5.	To realize using op-amps Inverting and Non-Inverting Zero Crossing Detectors.
6.	To designan op-amp Inverting Schmitt Trigger for given UTP and LTP.
7.	To realize using op-amp an Astable Multivibrator.
8.	To design and implement using op-amps a. Butterworth 1st and 2nd order Low pass filter b. Butterworth 1st and 2nd order High pass filter
9.	To design and implement using op-amp a. RC Phase Shift Oscillator b. Wein Bridge oscillator
10.	To design and implement Mono-stable Multivibrator using 555 timer
11.	To design and implement 4 - bit R-2R Digital to Analog Converter
12.	To design and implement voltage regulator using 7805 IC.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

The CIE marks for the theory component of the Integrated Course (IC) shall be 30 marks and for the laboratory component 20 marks.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY COMPONENT OF IC:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes / Weekly test / project work for (20+20) marks, scaled down to **20 marks.**
4. Total marks scored **(30+20 = 50 marks)** scaled down to **25.**

CIE FOR THE PRACTICAL COMPONENT OF IC:

1. On completion of every experiment / program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day.
2. Each experiment is evaluated for 10 marks and scaled down to **5 marks.**
3. Laboratory test at the end of the 15th week of the semester / after completion of all the experiments shall be conducted for **50 marks** and scaled down to **20 marks.**
4. Total marks scored for lab component: **05+20=25 marks**.
5. The minimum marks to be secured in CIE to appear for SEE shall be 10(40% of maximum marks 25) in the theory and 10(40% of Maximum marks 25) in the practical.
6. The laboratory component of the **integrated course** shall be CIE only. However, in SEE, the questions from the practical component shall be included.

Theory				
IA Test	**Exam conducted for**	**Scaled down to**	**Average of best two tests**	**Total**
IA-1	**50**	**30**	**30**	**50/2=25**
IA-2	**50**	**30**		
IA-3	**50**	**30**		
Two Assignments	**2×10=20**	**10**	**10**	
Two Quizzes	**2×10=20**	**10**	**10**	

LAB			
Continuous performance and record writing	**Each experiments evaluated for 10 marks**	**Scaled down to 05 marks**	**5+20=25**
Internal Test + Viva voce	**Exam conducted for 50 marks**	**Scaled down to 20 marks**	

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice. Students should answer five full questions, selecting one full question from each module.
5. Students have to answer for 100 marks and marks scored out of 100 shall be proportionally reduced to 50 marks.
6. The maximum marks from the practical component to be included in the SEE question paper is **16 marks.**
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	-	-	1	3	-	-	-	1	1	1
CO2	2	-	-	1	3	-	-	-	1	1	1
CO3	2	-	-	1	3	-	-	-	1	1	1
CO4	2	-	-	1	3	-	-	-	1	1	1
CO5	2	-	-	1	3	-	-	-	1	1	1

Level 3 - High, Level 2 - Moderate, Level 1 –Low

SEMESTER-III					
DIGITAL SYSTEM DESIGN USING VERILOG **Category: IPCC**					
Course Code	:	B24EC304	CIE	:	50 Marks
Teaching Hours/Week (L:T:P)	:	3:0:2	SEE	:	50 Marks
Total Hours	:	45(T)+15(P)	Total	:	100 Marks
Credits	:	4	SEE Duration	:	3 Hrs

Course Objectives	
1.	To study the concepts of simplifying Boolean expression using K-map techniques and Quine-Mc Cluskey minimization techniques.
2.	To study the concepts of designing and analyzing combinational logic circuits.
3.	To impart design methods and analysis of sequential logic circuits.
4.	To impart the concepts of Verilog HDL-data flow and behavioural models for the design of digital systems.
5.	To study the gate level modelling techniques using HDL.

Module – 1: Simplification of Boolean Expression	**No. of Hours**
Karnaugh maps-up to 4 variables, Quine-Mc Cluskey Minimization Technique. Quine-Mc Cluskey using Don't Care Terms. **(Chapter 4 Section 4.4, 4.5, 4.8 of Text1).** Logic design with MSI Components and Programmable logic devices: Binary adders and Subtracters, Decimal Adders, Comparators, Decoders, Encoders, Multiplexers. **(Chapter 5 Section 5.1 TO 5.6 -Text 1).**	9
Module – 2: Flip-Flops and its Applications	**No. of Hours**
Basic Bistable elements, Latches, The master-slave flip-flops (pulse-triggered flip-flops): SR flip-flops, JK flip-flops, Characteristic equations, Registers, binary ripple counters, and synchronous binary counters. **(Chapter 6 Section-6.1,6.2,6.4-6.8-Text-1)**	9
Module – 3: Sequential Circuit Design	**No. of Hours**
Design of a synchronous counter, Design of a synchronous mod-n counter using clocked JK, D, T and SR flip-flops. (Text 1 - Chapter 6 Section-6.9) **State Machines:** Mealy and Moore models, State machine notation, Construction of state diagrams. **(Text 2 - Chapter 6 – Section-6.1, 6.2,6.3)**	9
Module– 4: Hierarchical Modeling Concepts	**No. of Hours**
Design methodologies, 4-bit ripple carry counter, modules, instances, components of a simulation, example, design block, stimulus block **(Text3-Chapter2 Section 2.1 to 2.6)** **Basic Concepts:** Data types, System tasks and compiler directives **(Text3-Chapter3 Section 3.2,3.3)** **Modules and Ports:** Modules, list of ports, Port declaration **(Text3-Chapter4 Section4.1, 4.2.1, 4.2.2)**	9
Module– 5: Gate-Level Modeling	**No. of Hours**
Gate types - (Text2- Chapter5(5.1) **Dataflow Modeling:** Continuous Assignments, Expressions, Operators, and Operands, Operator types (Text3-Chapter6 Section 6.1,6.3,6.4) **Behavioral Modeling:** Structures procedures, Procedural Assignments (Text3-Chapter7Section7.1,7.2)	9

PRACTICAL COMPONENT OF IPCC

Using suitable hardware and simulation software, demonstrate the operation of the following circuits:

Sl. No	Experiments
1.	To simplify the given Boolean expressions and realize using Verilog program
2.	Write a Verilog program for the following combinational designs Encoder, decoder, multiplexer, de-multiplexer, comparator (Any 3 program)
3.	Write a Verilog code to describe the functions of a Full Adder using three modeling styles.
4.	To realize the following Code converters using Verilog Behavioral description. Binary to Gray, Binary to Excess-3
5.	To realize 4-bit ALU using Verilog program.
6.	Develop the Verilog code for the following flip-flops, SR, D, JK and T.
7.	To realize Counters - up/down (BCD and Binary) using Verilog Behavioral description.
Demonstration Experiments (For CIE only, not for SEE)	
8.	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
9.	Verilog programs to interface a Relay or ADC to the FPGA/CPLD and demonstrate its working.
10.	Verilog programs to interface DAC to the FPGA/CPLD for Waveform generation.
11.	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.
12.	Verilog programs to interface for a 4x4 keypad matrix.

Course Outcomes: At the end of the course, the students will be able to	
CO1	Apply the knowledge of Boolean functions to design combinational logic circuits. using K-map and Quine-McCluskey minimization technique
CO2	Analyze the concepts of Flip Flops(SR, D,T and JK)
CO3	Design the sequential circuits using SR, JK, D, T flip-flops and Mealy & Moore machines
CO4	Understand the fundamental concepts of Verilog HDL.
CO5	Apply the knowledge of Verilog HDL syntax to implement Combinational circuits and sequential circuits.

Text Books	
1.	Digital Principles and Design by Donald D Givone, McGrawHill, 2002.
2.	Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001.
3.	Verilog HDL-A Guide to Digital Design and Synthesis IEEE 1364-2001 Compliant by Samir Palnitkar

Reference Books	
1.	Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
2.	HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dream techpress. Impression 2019.
3.	Fundamentals of HDL,by Cyril PR, Pearson/Sanguine2010

Web links and Video lectures (e-Resources)
1.https://www.youtube.com/playlist?list=PLwdnzlV3ogoVlY7iVqr-FhWUQEX7JDdiP
2. Digital Systems Design Using Verilog - Charles Roth, Lizy K. John, ByeongKil Lee - Google Books

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

The CIE marks for the theory component of the Integrated Course (IC) shall be 30 marks and for the laboratory component 20 marks.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY COMPONENT OF IC:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes / Weekly test / project work for (20+20) marks, scaled down to **20 marks.**
4. Total marks scored **(30+20 = 50 marks)** scaled down to **25.**

CIE FOR THE PRACTICAL COMPONENT OF IC:

1. On completion of every experiment / program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day.
2. Each experiment is evaluated for 10 marks and scaled down to **5 marks.**
3. Laboratory test at the end of the 15th week of the semester / after completion of all the experiments shall be conducted for **50 marks** and scaled down to **20 marks.**
4. Total marks scored for lab component: **05+20=25 marks**.
5. The minimum marks to be secured in CIE to appear for SEE shall be 10(40% of maximum marks 25) in the theory and 10(40% of Maximum marks 25) in the practical.
6. The laboratory component of the **integrated course** shall be CIE only. However, in SEE, the questions from the practical component shall be included.

Theory				
IA Test	**Exam conducted for**	**Scaled down to**	**Average of best two tests**	**Total**
IA-1	**50**	**30**	**30**	**50/2=25**
IA-2	**50**	**30**		
IA-3	**50**	**30**		
Two Assignments	**2×10=20**	**10**	**10**	
Two Quizzes	**2×10=20**	**10**	**10**	

LAB			
Continuous performance and record writing	**Each experiments evaluated for 10 marks**	**Scaled down to 05 marks**	**5+20=25**
Internal Test + Viva voce	**Exam conducted for 50 marks**	**Scaled down to 20 marks**	

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.

4. **Part-B** contains total 10 questions. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice. Students should answer five full questions, selecting one full question from each module.
5. Students have to answer for 100 marks and marks scored out of 100 shall be proportionally reduced to 50 marks.
6. The maximum marks from the practical component to be included in the SEE question paper is **16 marks.**
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	-	3	1	3	-	-	-	-	1	1
CO2	3	1	3	1	3	-	-	-	-	1	1
CO3	3	1	3	1	3	-	-	-	-	1	1
CO4	2	-	2	1	3	-	-	-	-	1	1
CO5	2	-	2	1	3	-	-	-	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-III					
ANALOG AND DIGITAL ELECTRONICS LAB **Category: PCCL**					
Course Code	:	B24EC305L	CIE	:	50 Marks
Teaching Hours (L : T : P)	:	0 : 0 : 2	SEE	:	50 Marks
Total Hours	:	15(P)	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Objectives	
1.	Understand the electronic circuit schematic and it's working.
2.	Realize and test amplifier and oscillator circuits for the given specifications.
3.	Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
4.	Design and test the combinational and sequential logic circuits for their Functionalities
5.	Use the suitable ICs based on the specifications and functions.

Sl. No	**List of Experiments**
1.	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
2.	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator
3.	Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator
4.	Design and Test the second order Active Filters and plot the frequency response, i) Low pass and Highpass Filter ii) Bandpass and Bandstop Filter
5.	Design and test the following using 555 timer i) MonostableMultivibraator ii) AstableMultivibrator
6.	Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches (ii) by generating digital inputs using mod-16
7.	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor& Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX).
8.	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa.
9.	Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop
10.	Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.
11.	Design and implement Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop
12.	Realize a) Mod-N Counter using IC7490 / 7476 b) Synchronous counter using IC74192

Course Outcomes: At the end of the course, the students will be able to	
CO1	Design and analyze the BJT/FET amplifier and oscillator circuits.
CO2	Design and test Opamp circuits to realize the mathematical computations, DAC and precision rectifiers.
CO3	Design and test the combinational logic circuits for the given specifications.
CO4	Test the sequential logic circuits for the given functionality.
CO5	Demonstrate the basic electronic circuit experiments using 555 timer.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

Component	Scale down to	Total Marks
Conduction of experiments and Record Writing (Each Experiment evaluated for 10 marks)	20	20
Internal Lab Test 1(After 6 experiments) Exam conduction for 50 marks	15	15
Internal Lab Test 2 (After 6 experiments) Exam conduction for 50 marks	15	15
	CIE	**50**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Students can pick one question (experiment) from the questions lot prepared by the examiners.
4. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
5. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
6. Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	1	1	1	3	-	-	1	-	1	1
CO2	2	1	1	1	3	-	-	1	-	1	1
CO3	2	1	1	1	3	-	-	1	-	1	1
CO4	2	1	1	1	3	-	-	1	-	1	1
CO5	2	1	1	1	3	-	-	1	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 – Low

SEMESTER-III					
POWER ELECTRONICS **Category: ESC/ETC/PLC-III**					
Course Code	:	B24EC361	CIE	:	50 Marks
Teaching Hours L : T : P	:	3:0:0	SEE	:	50 Marks
Total Hours	:	45(T)	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Objectives	
1.	To learn the Classification of power electronic circuits.
2.	To study the different turn ON methods of power devices.
3.	To Study thyristor circuits with different triggering conditions.
4.	To Learn the applications of power devices in controlled rectifiers
5.	To Design of DC-DC converters and inverters.

Module – 1: Introduction	**No. of Hours**
Introduction -Applications of Power Electronics, Power Semiconductor Devices, Control Characteristics of Power Devices, types of Power Electronic Circuits, Peripheral Effects. Power Transistors: Power BJTs: Steady state characteristics. Power MOSFETs: device operation, switching characteristics, IGBTs: device operation, output and transfer characteristics, di/dt and dv/dt limitations. (Text 1) L1, L2	9
Module – 2: Thyristors	**No. of Hours**
Thyristors -Introduction, Principle of Operation of SCR, Static Anode-Cathode Characteristics of SCR, Two transisitor model of SCR, Gate Characteristics of SCR, Turn-ON Methods, Turn-OFF Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A and Class B types, Gate Trigger Circuit: Resistance Firing Circuit, Resistance capacitance firing circuit, UJT Firing Circuit. (Text 2) L1, L2, L3	9
Module – 3: Controlled Rectifiers	**No. of Hours**
Controlled Rectifiers -Introduction, Principle of Phase-Controlled Converter Operation, Single-Phase Full Converter with RL Load, Single-Phase Dual Converters, Single-Phase Semi Converter with RL load. AC Voltage Controllers -Introduction, Principles of ON-OFF Control, Principle of Phase Control, Single phase controllers with resistive and inductive loads. (Text 1) L1, L2, L3	9
Module – 4: DC-DC Converters	**No. of Hours**
DC-DC Converters -Introduction, principle of step-down operation and it‘s analysis with RL load, principle of step-up operation, Step-up converter with a resistive load, Performance parameters, Converter classification, Switching mode regulators: Buck regulator, Boost regulator, Buck-Boost Regulators, Chopper circuit design. (Text 1) L1, L2	9
Module – 5: Pulse Width Modulated Inverters	**No. of Hours**
Pulse Width Modulated Inverters-Introduction, principle of operation, performance parameters, Single phase bridge inverters, voltage control of single phase inverters, current source inverters, Variable DC-link inverter, Boost inverter, Inverter circuit design. (Text 1) L1, L2	9

Course Outcomes: At the end of the course, the students will be able to:	
CO1	Understand the characteristics of different power devices and identify the various applications associated with it.
CO2	Analyze the output response of a thyristor circuit with various triggering options.
CO3	Analyze the response of controlled rectifier with resistive and inductive loads.
CO4	Examine the operation of inverter circuit and static switches.
CO5	Understand the working of power circuit as DC-DC converter.

Text Books	
1.	Mohammad H Rashid, Power Electronics, Circuits, Devices and Applications, 3rd/4th Edition, Pearson Education Inc, 2014, ISBN: 978-93-325-1844-5.
2.	M.D Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897

Reference Books	
1.	L. Umanand, Power Electronics, Essentials and Applications, John Wiley India Pvt. Ltd, 2009.
2.	P.C. Sen, ―Modern Power Electronics‖, S Chand & Co New Delhi, 2005.

Web links and Video lectures (e-Resources)
1. Video Lectures | Power Electronics | Electrical Engineering and Computer Science | MIT Open Course Ware

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
5. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50).

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and it carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	-	2	-	-	-	1	-	-	1	1
CO2	3	-	2	-	-	-	1	-	-	1	1
CO3	3	-	2	-	-	-	1	-	-	1	1
CO4	3	-	2	-	-	-	1	-	-	1	1
CO5	3	-	2	-	-	-	1	-	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 – Low

SEMESTER-III					
SOLID STATE DEVICES **Category: ESC/ETC/PLC-III**					
Course Code	:	B24EC362	CIE	:	50 Marks
Teaching Hours (L : T : P)	:	3:0:0	SEE	:	50 Marks
Total Hours	:	45(T)	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Objectives	
1.	Understand the basics of semiconductor physics.
2.	Describe the mathematical models BJTs and FETs along with the constructional details.
3.	Understand the construction and working principles of optoelectronic devices.
4.	Understand the fabrication process of semiconductor devices and CMOS process integration.

Module – 1: Semiconductors	**No. of Hours**
Bonding forces in solids, Energy bands, Metals, Semiconductors and Insulators, Direct and Indirect semiconductors, Electrons and Holes, Intrinsic and Extrinsic materials, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility, Hall Effect. (Text1:3.1.1,3.1.2,3.1.3,3.1.4,3.2.1,3.2.3,3.2.4,3.4.1,3.4.2,3.4.3,3.4.5).	9
Module – 2 : PN Junctions	**No. of Hours**
Forward and Reverse biased junctions-Qualitative description of Current flow at a junction, reverse bias, Reverse bias breakdown- Zener breakdown, avalanche breakdown, Rectifiers.(Text1:5.3.1,5.3.3,5.4,5.4.1,5.4.2,5.4.3) Optoelectronic Devices Photodiodes: Current and Voltage in an Illuminated Junction, Solar Cells, Photodetectors. Light Emitting Diode: Light Emitting materials. (Text1:8.1.1,8.1.2,8.1.3,8.2,8.2.1),	9
Module – 3: Bipolar Junction Transistor	**No. of Hours**
Fundamentals of BJT operation, Amplification with BJTS,BJT Fabrication, The coupled Diode model(Ebers-Moll Model),Switching operation of a transistor, Cutoff, saturation, switching cycle, specifications, Drift in the base region, Base narrowing, Avalanche breakdown. (Text1:7.1,7.2,7.3,7.5.1,7.6,7.7.1,7.7.2, 7.7.3)	9
Module – 4: Field Effect Transistors	**No. of Hours**
Basic pn JFET Operation, Equivalent Circuit and Frequency Limitations, MOSFET-Two terminal MO S structure Energy band diagram, Ideal Capacitance -Voltage Characteristics and Frequency Effects, Basic MOSFET Operation- MOSFET structure, Current-Voltage Characteristics. (Text2:9.1.1, 9.4, 9.6.1, 9.6.2, 9.7.1, 9.7.2, 9.8.1, 9.8.2).	9
Module – 5: Fabrication of p-n junctions and Integrated Circuits	**No. of Hours**
Fabrication of p-n junctions Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion implantation, chemical vapour deposition, photolithography, Etching, metallization. (Text 1: 5.1) Integrated Circuits Background, Evolution of ICs, CMOS Process Integration, Integration of Other Circuit Elements.(Text 1:9.1,9.2,9.3.1,9.3.3).	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Analyse the principles of semiconductor Physics
CO2	Identify the mathematical models of BJT, and MOS transistors for circuits and systems.
CO3	Analyse the principles of optoelectronic devices.
CO4	Analyse the fabrication process of semiconductor devices

Text Books	
1.	Ben. G. Streetman, Sanjay Kumar Banerjee, "Solid State Electronic Devices",7th Edition,Pearson Education,2016,ISBN978-93-325-5508-2.
2.	Donald A Neamen, DhrubesBiswas, "Semiconductor Physics and Devices", 4th Edition,McGraw Hill Education, 2012,ISBN 978-0-07- 107010-2.

Reference Text Books	
1.	S.M.Sze,KwokK.Ng,"PhysicsofSemiconductorDevices",3rd Edition, Wiley,2018.
2.	AdirBar-Lev,"SemiconductorandElectronicDevices",3rd Edition,PHI, 1993
Web links and Video lectures (e-Resources)	
1. https://www.youtube.com/playlist?list=PLpe3qgeJLpB1ufieUIF6hY4gESxIOqZeF 2. https://archive.nptel.ac.in/courses/113/106/113106065/	

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
5. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50).

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and it carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	1	2	1	1	-	-	-	-	1	1
CO2	3	1	2	1	1	-	-	-	-	1	1
CO3	3	1	2	1	1	-	-	-	-	1	1
CO4	3	1	2	1	1	-	-	-	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-III					
COMPUTER ORGANIZATION AND ARCHITECTURE **Category: ESC/ETC/PLC-III**					
Course Code	:	B24EC363	CIE	:	50 Marks
Teaching Hours/Week (L:T:P: S)	:	3:0:0	SEE	:	50 Marks
Total Hours	:	45(T)	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Objectives	
1.	To make students understand the basic structure and operation of digital computer
2.	Describe arithmetic and logical operations with integer and floating-point operands.
3.	Describe memory hierarchy and concept of virtual memory.
4.	Illustrate organization of a simple processor, pipelined processor and other computing systems.
5.	To introduce the parallel processing technique

Module – 1: Basic Structure of Computer System	**No. of Hours**
Basics of a computer system: Evolution, Ideas, Technology, Performance, Power wall, Uniprocessors to Multiprocessors. Addressing and addressing modes. Instructions: Operations and Operands, Representing instructions, Logical operations, control operations.	9
Module – 2: Arithmetic Operations	**No. of Hours**
Numbers, Arithmetic Operations and Characters, Addition and Subtraction of Signed Numbers, Design of Fast Adders, Multiplication of Positive Numbers, Signed Operand Multiplication, Fast Multiplication, Integer Division.	9
Module – 3: Memory System	**No. of Hours**
Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage-Magnetic Hard Disks.	9
Module– 4: Basic Processing Unit	**No. of Hours**
Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Micro programmed Control.	9
Module– 5: Advanced Computer Architecture	**No. of Hours**
Parallel processing architectures and challenges, Hardware multithreading, Multicore and shared memory multiprocessors, Introduction to Graphics Processing Units, Clusters and Warehouse scale computers – Introduction to Multiprocessor network topologies.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Describe data representation, instruction formats and the operation of a digital computer
CO2	Explain different ways of accessing an input / output device including interrupts.
CO3	Illustrate the organization of different types of semiconductor and other secondary storage memories
CO4	Illustrate simple processor organization based on hardwired control and micro programmed control
CO5	Discuss parallel processing technique and unconventional architectures.

Text Books	
1.	David A. Patterson and John L. Hennessey, ―Computer Organization and Design‖, 5th edition, Morgan Kauffman / Elsevier, 2014. (UNIT I, V)
2.	Carl Hamacher, ZvonkoVranesic, SafwatZaky: Computer Organization, 5th Edition, Tata McGraw Hill, 2002.(Unit 2,3,4)

Reference Books	
1.	Govindarajalu, ―Computer Architecture and Organization, Design Principles and Applications", 2nd edition, McGraw-Hill Education India Pvt Ltd, 2014.
2.	William Stallings: Computer Organization & Architecture, 7th Edition, PHI, 2006.
3.	Vincent P. Heuring& Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

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CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
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SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and it carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
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CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
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CO2	3	1	1	1	2	2	-	-	-	2	1
CO3	3	1	1	1	2	1	-	-	-	3	1
CO4	3	1	1	1	2	2	-	-	-	2	1
CO5	3	1	1	1	2	1	-	-	-	3	1

Level 3 – High, Level 2 – Moderate, Level 1 – Low

SEMESTER-III					
OBJECT ORIENTED PROGRAMMING **Category: ESC/ETC/PLC-III** **(Common to ECE, RA)**					
Course Code	:	B24EC364	CIE	:	50 Marks
Teaching Hours/Week (L:T:P)	:	3:0:0	SEE	:	50 Marks
Total Hours	:	45(T)	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Objectives	
1.	To understand object-oriented programming using C++and Gain knowledge about the capability to store information together in an object
2.	To illustrate the capability of a class to rely upon another class and functions
3.	To Create and process data in files using file I/O functions
4.	To understand the process of templates and virtual attributes.
5.	To understand the generic programming features of C++ including Exception handling

Module– 1: An overview of C++	**No. of Hours**
What is object-Oriented Programming? Introducing C++ Classes, The General Form of a C++ Program. Classes and Objects: Classes, Friend Functions, Friend Classes, Inline Functions, Parameterized Constructors, Static Class Members, When Constructors and Destructors are Executed, The Scope Resolution Operator, Passing Objects to functions, Returning Objects, Object Assignment Ch 11, Ch 12	9
Module– 2: Arrays, Pointers, References, and the Dynamic Allocation Operators	**No. of Hours**
Arrays of Objects, Pointers to Objects, The this Pointer, Pointers to derived types, Pointers to class members. Functions Overloading, Copy Constructors: Functions Overloading, Overloading Constructor Functions. Copy Constructors, Default Function Arguments, Function Overloading and Ambiguity. Ch 13, Ch 14	9
Module– 3: Operator Overloading	**No. of Hours**
Creating a Member Operator Function, Operator Overloading Using a Friend Function, Overloading new and delete Inheritance: Base-Class Access Control, Inheritance and Protected Members, Inheriting Multiple Base Classes , Constructors, Destructors and Inheritance, Granting Access, Virtual Base Classes Ch 15, Ch 16	9
Module– 4: Virtual Functions and Polymorphism	**No. of Hours**
Virtual Functions, The Virtual Attribute is Inherited, Virtual Functions are Hierarchical, Pure Virtual Functions, Using Virtual Functions, Early v/s Late Binding. Templates: Generic Functions, Applying Generic Functions, Generic Classes. The type name and export Keywords. The Power of Templates Ch 17, Ch 18	9
Module– 5: Exception Handling	**No. of Hours**
Exception Handling Fundamentals, Handling Derived-Class Exceptions, Exception Handling Options, Applying Exception Handling. The C++ I/O System Basics: C++ Streams, The C++ Classes, Formatted I/O File I/O: and File Classes, Opening and Closing a File, Reading and Writing Text Files, Detecting EOF. Ch 19, Ch 20, Ch21	9

Course outcome: At the end of the course, the student will be able to	
CO1	Understand the basic concepts of object-oriented programming.
CO2	Design appropriate classes for the given real world scenario.
CO3	Apply the knowledge of compile-time / run-time polymorphism to solve the given problem
CO4	Use the knowledge of inheritance for developing optimized solutions
CO5	Apply the concepts of templates and exception handling for the given problem 6 Use the concepts of input output streams for file operations

Text Books	
1.	1. Herbert schildt, The Complete Reference C++, 4th edition, TMH, 2005

Reference Books	
1.	1. Balagurusamy E, Object Oriented Programming with C++, Tata McGraw Hill Education Pvt.Ltd., 6th Edition 2016.
2.	Bhave , " Object Oriented Programming With C++", Pearson Education , 2004.

Web links and Video lectures (e-Resources)
1. Basics of C++ - https://www.youtube.com/watch?v=BClS40yzssA
2. Functions of C++ -https://www.youtube.com/watch?v=p8ehAjZWjPw

ASSESSMENT DETAILS BOTH (CIE AND SEE)

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CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

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1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
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CO3	2	1	1	2	3	-	-	1	-	1	1
CO4	2	1	1	1	1	-	-	-	1	2	1
CO5	1	1	1	2	2	-	-	-	1	1	1

Level3 -High, Level2- Moderate, Level1- Low

SEMESTER-III					
C++ PROGRAMMING LAB **Category: AEC/SEC-III** **(Common to ECE, RA)**					
Course Code	:	B24EC381	CIE	:	50 Marks
Teaching Hours/Week (L:T:P)	:	0:0:2	SEE	:	50 Marks
Total Hours	:	15(P)	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Objectives	
1.	Understand object-oriented programming concepts, and apply them in solving problems..
2.	To create, debug and run simple C++ programs..
3.	Introduce the concepts of functions, friend functions, inheritance, polymorphism and function overloading
4.	Introduce the concepts of exception handling and multithreading
5.	Understand the concept of Inheritance

Sl. No	**Experiments**
1.	Write a C++ program to find largest, smallest & second largest of three numbers using inline functions Max & Min.
2.	Write a C++ program to calculate the volume of different geometric shapes like cube, cylinder and sphere using function overloading concept.
3.	Define a STUDENT class with USN, Name & Marks in 3 tests of a subject. Declare an array of 10 STUDENT objects. Using appropriate functions, find the average of the two better marks for each student. Print the USN, Name & the average marks of all the students.
4.	Write a C++ program to create class called MATRIX using two-dimensional array of integers, by overloading the operator == which checks the compatibility of two matrices to be added and subtracted. Perform the addition and subtraction by overloading + and – operators respectively. Display the results by overloading the operator r <<. . If (m1 == m2)then m3 = m1 +m2 and m4= m1 – m2 else display error
5	Demonstrate simple inheritance concept by creating a base class FATHER with data members: First Name, Surname, DOB & bank Balance and creating a derived class SON, which inherits: Surname & Bank Balance feature from base class but provides its own feature: First Name & DOB. Create & initialize F1 & S1 objects with appropriate constructors & display the FATHER & SON details.
6.	Write a C++ program to define class name FATHER & SON that holds the income respectively. Calculate & display total income of a family using Friend function.
7.	Write a C++ program to accept the student detail such as name & 3 different marks by get_data() method & display the name & average of marks using display() method. Define a friend function for calculating the average marks using the method mark_avg().
8.	Write a C++ program to explain virtual function (Polymorphism) by creating a base class polygon which has virtual function areas two classes rectangle & triangle derived from polygon & they have area to calculate & return the area of rectangle & triangle respectively
9.	Design, develop and execute a program in C++ based on the following requirements: An EMPLOYEE class containing data members &members functions: i) Data members: employee number (an integer), Employee_ Name (a string of characters), Basic_ Salary (in integer), All_ Allowances (an integer), Net_Salary (an integer). (ii) Member functions: To read the data of an employee, to calculate Net_Salary& to print the

	values of all the data members. (All_Allowances = 123% of Basic, Income Tax (IT) =30% of gross salary (=basic_ Salary_All_Allowances_IT).
10.	Write a C++ program with different class related through multiple inheritance & demonstrate the use of different access specified by means of members variables & members functions.
11.	Write a C++ program to create three objects for a class named count object with data members such as roll no. & Name. Create members function members data ( ) for setting the data values & display ( ) member functions to display which object has invoked it using,,this" pointer.
12.	Write a C++ program to implement exception handling with minimum 3 exceptions classes including two built in exceptions.

Course Outcomes: At the end of the course, the students will be able to	
CO1	Write C++ program to solve simple and complex problems
CO2	Apply and implement major object-oriented concepts like message passing, function overloading, operator overloading and inheritance to solve real-world problems.
CO3	Use major C++ features such as Templates for data type independent designs and File I/O to deal with large data set
CO4	Analyze, design and develop solutions to real-world problems applying OOP concepts of C++

ASSESSMENT DETAILS BOTH (CIE AND SEE)

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CONTINUOUS INTERNAL EVALUATION (CIE)

Component	Scale down to	Total Marks
Conduction of experiments and Record Writing (Each Experiment evaluated for 10 marks)	20	20
Internal Lab Test 1(After 6 experiments) Exam conduction for 50 marks	15	15
Internal Lab Test 2 (After 6 experiments) Exam conduction for 50 marks	15	15
	CIE	**50**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Students can pick one question (experiment) from the questions lot prepared by the examiners.
4. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
5. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
6. Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero. The minimum duration of SEE is 03 hours.

SEMESTER-III					
IOT FOR SMART INFRASTRUCTURE **Category: AEC/SEC-III**					
Course Code	:	B24EC382	CIE	:	50 Marks
Teaching Hours/Week(L:T:P)	:	1:0:0	SEE	:	50 Marks
Total Hours	:	15(T)	Total	:	100 Marks
Credits	:	1	SEE Duration	:	1Hrs

Course Objectives	
1.	To provide an understanding of the concepts, principles, and applications of IoT in the context of smart infrastructure.
2.	To explore the role of IoT technologies in transforming infrastructure into smart, efficient, and sustainable systems and analyse the challenges, opportunities, and considerations in implementing IoT for smart infrastructure..
3.	To examine real-world case studies and successful implementations of IoT in smart cities, buildings, transportation, and energy management and explore future trends and emerging technologies shaping the field of IoT for smart infrastructure

Module– 1: Introduction to IoT and Smart Infrastructure	**No. of Hours**
Introduction to IoT: Definition of IoT and its basic components, Overview of IoT applications in various industries, Importance of IoT in transforming infrastructure. Smart Infrastructure Overview: Introduction to smart infrastructure and its key components, Benefits and challenges of implementing smart infrastructure, Case studies showcasing successful smart infrastructure projects. IoT Technologies for Smart Infrastructure: Sensors and actuators: Types, functionalities, and applications; Communication protocols: Wi-Fi, Bluetooth, cellular networks, and their use in IoT; Cloud computing and data analytics in IoT for infrastructure; Edge computing: Real-time decision-making at the edge. Security and Privacy in IoT for Smart Infrastructure: Security challenges and threats in IoT, Privacy considerations and data protection in smart infrastructure, best practices and solutions for ensuring IoT security and privacy.	3
Module– 2: IoT Applications in Smart Cities	**No. of Hours**
Introduction to Smart Cities - Definition and key features of smart cities, Role of IoT in transforming cities into smart cities, Benefits and challenges of smart city implementations. IoT Applications in Smart City Infrastructure - Smart transportation: Intelligent traffic management and transportation systems, Smart buildings: Energy management and occupant comfort; Smart grids: Optimizing energy distribution and consumption; Waste management, water management, and environmental monitoring. Case Studies of Smart City Implementations: Showcase of successful smart city projects around the world; Analysis of the IoT technologies and strategies implemented; Lessons learned from these case studies. Future Trends in Smart Cities: Emerging technologies shaping the future of smart cities, Role of IoT, AI, and 5G in advancing smart city infrastructure, Opportunities and challenges for future smart city developments.	3
Module– 3: IoT Applications in Smart Buildings	**No. of Hours**
Introduction to Smart Buildings: Definition and key features of smart buildings, Benefits of IoT in improving energy efficiency and occupant comfort, Challenges and considerations in implementing smart building technologies. IoT Technologies for Smart Buildings: Building automation systems and controls; Energy management and monitoring using IoT devices; Indoor environmental quality monitoring and optimization; Smart lighting and HVAC systems. Case Studies of Smart Building Implementations: Showcase of successful smart building projects; Analysis of IoT technologies and solutions deployed; Lessons learned from these case studies. Future Trends in Smart Buildings: Emerging technologies for smart buildings; Integration of IoT with AI and machine learning; Potential impact of 5G on smart building applications.	3
Module– 4	**No. of Hours**
IoT Applications in Smart Buildings Introduction to Smart Buildings: Definition and key features of smart buildings, Benefits of IoT in improving energy efficiency and occupant comfort, Challenges and considerations in implementing smart building technologies. IoT Technologies for Smart Buildings: Building automation systems and controls; Energy management and monitoring using IoT devices; Indoor environmental quality monitoring and optimization; Smart lighting and HVAC systems. Case Studies of **Smart Building Implementations**: Showcase of successful smart building projects; Analysis of IoT technologies and solutions deployed; Lessons learned from these case	3

studies. Future Trends in Smart Buildings: Emerging technologies for smart buildings; Integration of IoT with AI and machine learning; Potential impact of 5G on smart building applications. Case Studies of Smart Transportation Implementations: Showcase of successful smart transportation projects; Analysis of IoT technologies and solutions deployed; Lessons learned from these case studies. Future Trends in Smart Transportation: Emerging technologies shaping the future of smart transportation; Role of IoT, AI, and autonomous vehicles; Potential impact of 5G on smart transportation applications.	
Module– 5: IoT for Smart Grids and Energy Management	**No. of Hours**
Introduction to Smart Grids: Definition and key features of smart grids: Role of IoT in optimizing energy distribution and consumption; Benefits and challenges of smart grid implementations. IoT Technologies for Smart Grids: Smart meters and energy monitoring devices; Demand response and load management; Grid optimization and fault detection using IoT; Renewable energy integration and grid stability. Case Studies of Smart Grid Implementations: Showcase of successful smart grid projects, Analysis of IoT technologies and solutions deployed, Lessons learned from these case studies. Future Trends in Smart Grids and Energy Management: Emerging technologies for smart grids; Integration of IoT, AI, and blockchain in energy management; Potential impact of 5G on smart grid applications.	3

Course Outcomes: At the end of the course, the students will be able to	
CO1	Define and explain the core concepts and components of IoT and its relevance to smart infrastructure. Identify and evaluate the key technologies and communication protocols used in IoT for smart infrastructure.
CO2	Assess the benefits, challenges, and ethical considerations associated with implementing IoT in smart infrastructure projects and analyse & compare different IoT applications in smart cities, buildings, transportation, and energy management.
CO3	Examine real-world case studies of successful IoT implementations in smart infrastructure and extract lessons learned. Demonstrate an understanding of security and privacy considerations in IoT for smart infrastructure.
CO4	Discuss the impact of emerging technologies, such as artificial intelligence and 5G, on the future of IoT in smart infrastructure. Apply knowledge and critical thinking skills to propose IoT-based solutions for smart infrastructure challenges.
CO5	Work effectively in teams to analyse, design, and present IoT projects related to smart infrastructure and communicate effectively and articulate the potential benefits and limitations of IoT for smart infrastructure.

Web links and Video Lectures (e-Resources):

- makes.mindmatrix.io

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Sensor Deployment and Data Collection: Organize a hands-on activity where participants work in groups to deploy sensors in a simulated smart infrastructure environment.
- Smart City Simulation Game: Develop a simulation game where participants take on different roles representing stakeholders in a smart city.
- IoT Solution Design Challenge: Assign participants to design an IoT-based solution for a specific smart infrastructure problem. They can work individually or in teams to identify the problem, propose an IoT solution, outline the required components and technologies, and create a prototype or presentation.
- Security and Privacy Risk Assessment: Conduct a group activity where participants analyse the security and privacy risks associated with IoT deployments in smart infrastructure.
- Field Visit to Smart Infrastructure Project: Organize a field visit to a smart infrastructure project, such as a smart building, smart city district, or IoT-enabled transportation system.

ASSESSMENT DETAILS (BOTH CIE AND SEE)

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CONTINUOUS INTERNAL EVALUATION (CIE)

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1. Three tests each of 50 marks (Multiple Choice Questions), after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
5. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50).

SEMESTER END EXAMINATION (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is 01 hour. The student has to secure a minimum of 35% of the maximum marks meant for SEE.

SEMESTER-III					
LAB VIEW PROGRAMMING **Category: AEC/SEC-III**					
Course Code	:	B24EC383	CIE	:	50 Marks
Teaching Hours L : T : P	:	0 : 0 : 2	SEE	:	50 Marks
Total Hours	:	15(P)	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Objectives	
1.	Understanding Virtual Instrument concepts and data acquisition operation
2.	Creating Virtual Instruments for practical works.

Sl. No	**List of Experiments** **PROGRAMMING**
1.	Basic arithmetic & logical operations
2.	Sum/Factorial of 'n' numbers using 'for' loop
3.	Build a Virtual Instrument that simulates a Water Level Detector.
4.	Programming exercises for loops in virtual instrumentation-Continuous Monitoring of Temperature.
5.	Programming exercises for graphs- Display Random Number into 3 different CHARTS (STRIP, SLOPE, SWEEP) and understand the difference between these in the UI. 4
6.	Programming Exercises on case and sequence structures:-Design the simple Calculator, making use of the inherent GUI present in the virtual instrumentation software.
7.	Programming Exercises on Arrays– Take a 2Darray input from the user and perform various array(and matrix) manipulations on it
8.	Programming Exercises on File Input output System – Read and write from ASCII and TDMS file
9.	Real time temperature acquisition and continuous monitoring using Virtual Instrumentation
INTERFACING	
10.	Developing voltmeter using DAQ cards – Acquiring a voltage and displaying it on a 'meter' indicator on the UI, thus designing a voltmeter
11.	Developing Signal Generator using DAQ Card – Using analog output; amplitude, shape and frequency controlled by user
12.	Develop Real time Temperature control using Thermistor

Course Outcomes: At the end of the course, the students will be able to	
CO1	To create data acquisition, analysis and display operations using LabVIEW
CO2	Create user interfaces with charts, graph and buttons
CO3	To develop the programming structures and data types that exist in LabVIEW
CO4	Use various editing and debugging techniques.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

Component	Scale down to	Total Marks
Conduction of experiments and Record Writing (Each Experiment evaluated for 10 marks)	20	20
Internal Lab Test 1(After 6 experiments) Exam conduction for 50 marks	15	15
Internal Lab Test 2 (After 6 experiments) Exam conduction for 50 marks	15	15
	CIE	**50**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Students can pick one question (experiment) from the questions lot prepared by the examiners.
4. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
5. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
6. Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3	-	3	-	-	-	-	-	-	1
CO2	2	1	3	-	3	-	-	-	-	-	-	1
CO3	2	1	3	-	3	-	-	-	-	-	-	1
CO4	2	1	3	-	3	-	-	-	-	-	-	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-III					
DATA STRUCTURES USING C **Category: AEC/SEC-III**					
Course Code	:	B24EC384	CIE	:	50 Marks
Teaching Hours L : T : P	:	0 : 0 : 2	SEE	:	50 Marks
Total Hours	:	15(P)	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Objectives	
1.	Understand basics of C programming language
2.	Acquire knowledge of - Various types of data structures, operations and algorithms - Sorting and searching operations
3.	Analyze the performance of - Stack, Queue, Lists, Trees, Hashing, Searching and Sorting techniques
4.	Implement all the applications of Data structures in a high-level language
5.	Acquire knowledge to design data structures for solving computing problems.

Sl. No	**List of Experiments**
1.	Write a C Program to create a Student record structure to store, N records, each record having the structure shown below: USN, Student Name and Semester. Write necessary functions a. To display all the records in the file. b. To search for a specific record based on the USN. In case the record is not found, suitable message should be displayed. Both the options in this case must be demonstrated. (Use pointer to structure for dynamic memory allocation) .
2.	Write a C Program to construct a stack of integers and to perform the following operations on it: a. Push b. Pop c. Display The program should print appropriate messages for stack overflow, stack underflow, and stack empty.
3.	Write a C Program to convert and print a given valid parenthesized infix arithmetic expression to postfix expression. The expression consists of single character operands and the binary operators + (plus), - (minus), * (multiply) and / (divide).
4.	Write a C Program to simulate the working of a queue of integers using an array. Provide the following operations: a. Insert b. Delete c. Display
5.	Write a C Program using dynamic variables and pointers to construct a stack of integers using singly linked list and to perform the following operations: a. Push b. Pop c. Display The program should print appropriate messages for stack overflow and stack empty.
6.	Write a C Program to support the following operations on a doubly linked list where each node consists of integers: a. Create a doubly linked list by adding each node at the front b. Insert a new node to the left of the node whose key value is read as an input c. Delete the node of a given data, if it is found, otherwise display appropriate message. d. Display the contents of the list. (Note: Only either (a,b and d) or (a, c and d) may be asked in the examination)
7.	Write a C Program a. To construct a binary search tree of integers. b. To traverse the tree using all the methods i.e., inorder, preorder and postorder. c. To display the elements in the tree.
8.	Write recursive C Programs for a. Searching an element on a given list of integers using the Binary Search method. b. Solving the Towers of Hanoi problem.
9.	Write a program to traverse a graph using BFS method. Write a program to check whether given graph is connected or not using DFS method.
10.	Design and develop a program in C that uses Hash Function H:K->L as H(K)=K mod m(reminder method) and implement hashing technique to map a given key K to the address space L. Resolve the collision (if any) using linear probing

Text Book(S)

1. Reema Thareja, Data Structures using C, 3rd Ed, Oxford press, 2012.

Reference Book(S):

1. Yedidyah, Augenstein, Tannenbaum: Data Structures Using C and C++, 2nd Edition, Pearson Education, 2003.
2. 2. Data Structures, Seynour Lipschutz and GAV Pai, Schaum's Outlines, McGraw Hill, 2008

Course Outcomes: At the end of the course, the students will be able to	
CO1	Understand basics of C programming language
CO2	Acquire knowledge of - Various types of data structures, operations and algorithms - Sorting and searching operations
CO3	Analyze the performance of - Stack, Queue, Lists, Trees, Hashing, Searching and Sorting techniques
CO4	Implement all the applications of Data structures in a high-level language
CO5	Design and apply appropriate data structures for solving computing problems.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

Component	Scale down to	Total Marks
Conduction of experiments and Record Writing (Each Experiment evaluated for 10 marks)	20	20
Internal Lab Test 1(After 6 experiments) Exam conduction for 50 marks	15	15
Internal Lab Test 2 (After 6 experiments) Exam conduction for 50 marks	15	15
	CIE	**50**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Students can pick one question (experiment) from the questions lot prepared by the examiners.
4. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
5. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
6. Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	-	-	-	3	-	-	-	-	1	-	1
CO2	2	-	-	-	3	-	-	-	-	1	-	1
CO3	2	1	-	-	3	-	-	-	-	1	-	1
CO4	2	1	-	-	3	-	-	-	-	1	-	1
CO5	2	1	-	-	3	-	-	-	-	1	-	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

IV - Semester Syllabus

SEMESTER-IV					
MATHEMATICS-IV FOR EC **Category: PCC**					
Course Code	:	B24ME401	CIE	:	50 Marks
Teaching Hours L : T : P	:	3:0:0	SEE	:	50 Marks
Total Hours	:	45(T)	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Objectives	
1.	Compute the solution by applying the acquired knowledge of linear algebra to the problems of engineering applications.
2.	To Provide the principles of statistical inferences with emphasison some commonly encountered hypotheses.
3.	To Provide the basics of hypothesis testing with emphasison some commonly encountered hypotheses.
4.	To develop mathematical model to integrate some non integrable functions using special theorems.
5.	To perform complex variables and to apply in signal transformation .

Module-1: Linear Algebra - II	**No. of Hours**
Inner Products, orthogonal matrices, orthogonal and ortho normal bases, Gram-Schmidt process, QR-factorization. Eigen values and Eigen vectors (recapitulation), diagonalization of a matrix (symmetric matrices) and singular value decomposition. **Application:** structural engineering to analyze vibrations and dynamic systems, computer graphics,	9
Module-2: StatisticalInference1	**No. of Hours**
Introduction, sampling distribution, standard error, testing of hypothesis, levels of significance, test of significances, confidence limits, simple sampling of attributes, test of significance for large samples, comparison of large samples. **Application:** Hypothesis testing and confidence intervals.	9
Module 3: StatisticalInference2	**No. of Hours**
Sampling variables, central limit theorem and confidences limit for unknown mean. Test of Significance for means of two small samples, students't' distribution, Chi-square distribution as a test of goodness of fit. F-Distribution. **Application:** Hypothesis testing	9
Module-4: Complex Variable-I	**No. of Hours**
Review of a function of a complex variable, limits, continuity, and differentiability. Analytic function and connected theorem and properties, Cauchy-Riemann equations in Cartesian and polar forms. Transformations: Conformal transformations, discussion of transformations: $w = z^2$, $w = e^z$ and bilinear transformations-problems. **Application:** Analyzing alternating current (AC) circuits, signal processing.	9
Module-5: Complex Variable-II	**No. of Hours**
Complex line integral ,properties of Complex line integral, Cauchy's theorem ,consequences of cauchy's theorem, cauchy's integral formula, generalized cauchy's integral formula, Laurent's theorem-Laurent's series , singularity and Residue, formulae for the residue at the pole, Cauchy's Residue theorem (without proof) and problems. **Application:** Calculating electric and magnetic fields, Fluid Dynamics.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Compute the solution by applying the acquired knowledge of linear algebra to the problems of image processing.
CO2	To solve the business related problems.
CO3	Use statistical methodology and tools in the decision making process.
CO4	Understand the concept of complex variables and their applications in signal transformation.
CO5	Demonstrate the ideas of complex differentiation and integration for solving related problems through theoretical approach.

Text Books	
1.	**RonaldE.Walpole,Raymond HMyers,SharonLMyers&KeyingYe**"Probability&Statistics for Engineers & Scientists",Pearson Education, 9th edition, 2017.
2.	**S.P Guptha** "Statistical Methods" ,Sultan Chand & Sons ,46th edition

Reference Text Books	
1.	**ErwinKreyszig**, "AdvancedEngineering Mathematics", John Wiley &Sons,9th Edition,2006.
2.	**B.S.Grewal**" Higher EngineeringMathematics",Khannapublishers,44th Ed.,2021.
3.	**GHaribaskaran**"Probability,QueuingTheory&ReliabilityEngineering",LaxmiPublication,Latest Edition, 2006

Web links and Video lectures (e-Resources)
1.https://nptel.ac.in/courses/12286025 2.VTUEDUSATPROGRAMME –20 3.http://www.class-central.com/subject/math(MOOCs)

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
5. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50).

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and it carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO8	PO11
CO1	3	3	3	2	-	-	-	-	1	-	2
CO2	3	3	3	2	-	-	-	-	1	-	2
CO3	3	3	3	2	-	-	-	-	1	-	2
CO4	3	3	3	2	-	-	-	-	-	-	2
CO5	3	3	3	2	-	-	-	-	-	-	2

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-IV					
ELECTROMAGNETIC FIELD THEORY **Category: PCC**					
Course Code	:	B24EC402	CIE	:	50 Marks
Teaching Hours/Week (L:T:P: S)	:	3:0:0	SEE	:	50 Marks
Total Hours	:	45(T)	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Objectives	
1.	To prepare students with fundamental knowledge of electrostatics.
2.	To introduce the concepts and laws related to static magnetic fields.
3.	To equip students with a basic foundation in Maxwell's Equations.
4.	To introduce the concept of Wave propagation in various mediums.

Module– 1: Electrostatics	**No. of Hours**
Introduction: Review of vector calculus, Coordinate systems. Coulomb's Law in Vector Form, Electric Field Intensity, Electric Flux Density T1: 1.1 – 1.9, 2.1 –2.2, 2.4 – 2.5, 3.1	9
Module– 2: Electrostatics (Contd..)	**No. of Hours**
Gauss Law –Applications- Charge distributions-line, surface, volume. Divergence of a vector and Divergence theorem, Maxwell's First equation (Electrostatics) Energy expended or work done in moving a point charge in anElectric field, The line integral, Electric current – Current density – continuity equation for current T1: – 3.2 - 3.3, 3.4.2, 3.4.3, 3.5, 4.1, 4.2, 5.1, 5.2	9
Module– 3: Magneto statics	**No. of Hours**
Poisson's and Laplace's equation, Examples of the solution of Laplace's equation Steady Magnetic field, Biot-Savart's law, Ampere's Circuital law, Curl & Stokes Theorem, Magnetic flux, Magnetic flux density. T1:6.6,6.7,7.1,7.2.1, 7.2.2, 7.2.3, 7.2.4, 7.3, 7.4, 7.5	9
Module– 4: Time Varying Field	**No. of Hours**
Force On A Moving Charge, Force on differential current elements, Force between differential current elements, Numerical problems, Magnetic Boundary conditions, Numerical problems Faraday's law, Displacement current, Limitations of Ampere's law, Maxwell's equations, T1: 8.1,8.2,8.3,8.7,9.1, 9.2, 9.3, 9.4	9
Module– 5: Uniform Plane Wave	**No. of Hours**
Uniform Plane Wave: Wave propagation in free space, Wave Propagation in Dielectric, Conducting Media, Poynting theorem and Wave power, Propagation in Good Conductors T1: 11.1, 11.2.1, 11.2.2, 11.3, 11.4	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Apply the concept of electrostatics to measure Electric Force, Field Intensity, Flux density, Total charge
CO2	Understand the concepts of Laplace & Poisson's Equation, and the applications of Electrostatics.
CO3	Apply the concept of magnetostatics to measure Magnetic Force, Field Intensity, Flux density Vector magnetic Potential and Boundary conditions.
CO4	Apply Maxwell's Equations on Time varying field problems.
CO5	Assess the Wave propagation in various mediums.

Text Books	
1.	"Engineering Electromagnetics", William H HaytJr, J.A. Buck, 9th Edition, Tata McGraw Hill, 2006, Special Indian Edition 2014.
2.	'Principles of Electromagnetics", Matthew N. O. Sadiku, S. V. Kulkarni, 6th Edition, Oxford University Press, 2007, 6th Impression 2018.

Reference Books	
1.	"Electromagnetic waves and radiating systems", Edward C Jordan, Keith G Balmain, , 2nd Edition PHI, 2005.
2.	"Electromagnetics and Applications" John D. Kraus, 2nd Edition
3.	"Elements of Engineering Electromagnetics" NannapaneniNarayanaRao, 6thEdition, Pearson Education.
4.	"Principles of Electromagnetics"Sadiku and Kulkarni, 6th Edition Oxford University Press 2015.

Web links and Video lectures (e-Resources)
1. https://nptel.ac.in/courses/108106073/
2. http://qeee.in/coursepack/generate_books/generated_books/1975/

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
5. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50).

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and it carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	1	1	2	1	-	-	-	-	1	1
CO2	3	1	1	2	1	-	-	-	-	1	1
CO3	3	1	1	2	1	-	-	-	-	1	1
CO4	3	1	1	2	1	-	-	-	-	1	1
CO5	3	1	1	2	1	-	-	-	-	1	1

Level-1-High, Level-2-Moderate, Level-3-Low

SEMESTER-IV					
COMMUNICATION SYSTEMS -I **Category: IPCC**					
Course Code	:	B24EC403	CIE	:	50 Marks
Teaching Hours L:T:P	:	3:0:2	SEE	:	50 Marks
Total Hours	:	45(T)+15(T)	Total	:	100 Marks
Credits	:	4	SEE Duration	:	3 Hrs

Course Objectives	
1.	Understand and analyze concepts of Analog Modulation schemes viz; AM, FM
2.	Design and analyze the electronic circuits for AM and FM modulation and demodulation.
3.	Evolve the concept of SNR in the presence of channel induced noise and Receiver Performance of Modulation Techniques
4.	Understand and Apply the concepts of digitization of signals.
5.	Design and evaluate the baseband transmission of PAM signals.

Module – 1: Amplitude Modulation	**No. of Hours**
AMPLITUDE MODULATION: Introduction, Amplitude Modulation: Time & Frequency Domain description, Switching modulator, Envelop detector. **DOUBLE SIDE BAND-SUPPRESSED CARRIERMODULATION:** Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing. **SINGLE SIDE-BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION:** SSB Modulation, VSB Modulation, Frequency Translation, Frequency- Division Multiplexing, Theme Example: VSB Transmission of Analog and Digital Television.	9
Module – 2: Angle Modulation	**No. of Hours**
ANGLE MODULATION: Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase-Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM Systems. The Superheterodyne Receiver	9
Module – 3: Noise in Analog Modulation	**No. of Hours**
NOISE - Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth (5.10 in Text) **NOISE INANALOG MODULATION:** Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Pre-emphasis and De-emphasis in FM.	9
Module – 4: Sampling and Quantization	**No. of Hours**
SAMPLING AND QUANTIZATION: Introduction, Why Digitize Analog Sources? The Low pass Sampling process Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves. The Quantization Process, Quantization Noise, Pulse-Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding,	9
Module – 5: Sampling and Quantization (Contd)	**No. of Hours**
Baseband Transmission of Digital signals: Introduction, Intersymbol Interference, Eye Pattern, Nyquist criterion for distortionless Transmission, Baseband M-ary PAM Transmission.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Analyze the principles and performance of analog modulation techniques such as Amplitude Modulation (AM) and Frequency Modulation (FM).
CO2	Design and evaluate modulation and demodulation circuits for AM and FM systems using appropriate electronic components.
CO3	Assess the effect of channel-induced noise on signal quality and evaluate receiver performance using Signal-to-Noise Ratio (SNR) metrics for various analog modulation schemes.
CO4	Apply the concepts of signal sampling, quantization, and encoding in the digitization of analog signals.
CO5	Design and analyze baseband transmission systems using Pulse Amplitude Modulation (PAM), and evaluate their performance under ideal and noisy conditions.

Text Books	
1.	"Communication Systems", Simon Haykin & Moher, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978-81-265-2151
2.	"Modem Digital and Analog Communication Systems", B. P. Lathi, Oxford University Press, 4th edition

Reference Text Books	
1.	An Introduction to Analog and Digital Communication, Simon Haykin, John Wiley India Pvt. Ltd., 2008, ISBN 978-81-265-3653-5
2.	Principles of Communication Systems, H. Taub & D. L. Schilling, TMH, 2011.
3.	Communication Systems, Harold P.E, Samy A. Mahmoud, Lee Elliott Stern, Pearson Edition, 2004.

Web links and Video lectures (e-Resources)
1. **https://nptel.ac.in/courses/108104091**
2. **https://nptel.ac.in/courses/117102059**

LABORATORY

Practical Component of IPCC (12 Experiments)

Sl. No	Name of the experiment
1.	Basic Signals and Signal Graphing: a) unit Step, b) Rectangular, c) standard triangle d) sinusoidal and e) Exponential signal.
2.	Illustration of signal representation in time and frequency domains for a rectangular pulse.
3.	Amplitude Modulation and demodulation: Generation and display the relevant signals and its spectrums.
4.	Frequency Modulation and demodulation: Generation and display the relevant signals and its spectrums.
5.	Sampling and reconstruction of low pass signals. Display the signals and its spectrum.
6.	Time Division Multiplexing and demultiplexing.
7.	PCM Illustration: Sampling, Quantization and Encoding
8.	Generate a)NRZ, RZ and Raised cosine pulse, b) Generate and plot eye diagram
9.	Generate the Probability density function of Gaussian distribution function.
10.	Display the signal and its spectrum of an audio signal.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

The CIE marks for the theory component of the Integrated Course (IC) shall be 30 marks and for the laboratory component 20 marks.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY COMPONENT OF IC:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes / Weekly test / project work for (20+20) marks, scaled down to **20 marks.**
4. Total marks scored **(30+20 = 50 marks)** scaled down to **25.**

CIE FOR THE PRACTICAL COMPONENT OF IC:

1. On completion of every experiment / program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day.
2. Each experiment is evaluated for 10 marks and scaled down to **5 marks.**
3. Laboratory test at the end of the 15th week of the semester / after completion of all the experiments shall be conducted for **50 marks** and scaled down to **20 marks.**
4. Total marks scored for lab component: **05+20=25 marks**.
5. The minimum marks to be secured in CIE to appear for SEE shall be 10(40% of maximum marks 25) in the theory and 10(40% of Maximum marks 25) in the practical.
6. The laboratory component of the **integrated course** shall be CIE only. However, in SEE, the questions from the practical component shall be included.

Theory				
IA Test	**Exam conducted for**	**Scaled down to**	**Average of best two tests**	**Total**
IA-1	**50**	**30**	**30**	**50/2=25**
IA-2	**50**	**30**		
IA-3	**50**	**30**		
Two Assignments	**2×10=20**	**10**	**10**	
Two Quizzes	**2×10=20**	**10**	**10**	

LAB			
Continuous performance and record writing	**Each experiments evaluated for 10 marks**	**Scaled down to 05 marks**	**5+20=25**
Internal Test + Viva voce	**Exam conducted for 50 marks**	**Scaled down to 20 marks**	

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice. Students should answer five full questions, selecting one full question from each module.
5. Students have to answer for 100 marks and marks scored out of 100 shall be proportionally reduced to 50 marks.
6. The maximum marks from the practical component to be included in the SEE question paper is **16 marks.**
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	3	1	3	3	-	-	1	1	2	1
CO2	2	2	1	2	3	-	-	1	1	2	1
CO3	2	2	1	1	2	-	-	1	1	2	1
CO4	2	2	1	2	2	-	-	1	1	2	1
CO5	2	1	1	3	2	-	-	1	1	2	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-IV					
CONTROL ENGINEERING **Category: IPCC**					
Course Code	:	B24EC404	CIE	:	50 Marks
Teaching Hours L : T : P	:	3:0:2	SEE	:	50 Marks
Total Hours	:	45(T)+15(P)	Total	:	100 Marks
Credits	:	4	SEE Duration	:	3 Hrs

Course Objectives	
1.	To understand basics of control systems. and design mathematical models.
2.	To understand the techniques of block diagram reduction and Signal Flow Graph.
3.	To Understand time domain and frequency domain analysis .
4.	To analyse the stability of a system from the transfer function.
5.	To study about the state space model of the system.

Module – 1: Introduction to Control Systems	**No. of Hours**
Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems - Mechanical Systems, Electrical Systems, Analogous Systems. Text 1: 1.1, 2.2	9
Module – 2 : Block diagrams and signal flow graphs	**No. of Hours**
Transfer functions, Block diagram algebra and Signal Flow graphs. Text1: 2.4, 2.5, 2.6	9
Module – 3: Time Response of feedback control systems	**No. of Hours**
Standard test signals, Unit step response of First and Second order Systems. Time response specifications, Time response specifications of second order systems, steady state errors and error constants. Introduction to PI, PD and PID Controllers (excluding design). Text1: 5.3, 5.4, 5.5	9
Module – 4: Stability analysis and Root Locus Techniques	**No. of Hours**
Concepts of stability, Necessary conditions for Stability, Routh stability criterion, Relative stability analysis: more on the Routh stability criterion. The root locus concepts, Construction of root loci. Text1: 6.1, 6.2, 6.4, 6.5, 7.1, 7.2, 7.3	9
Module – 5: Frequency domain analysis and stability	**No. of Hours**
Correlation between time and frequency response, Bode Plots, Experimental determination of transfer function. Mathematical preliminaries, Nyquist Stability criterion, (Stability criteria related to polar plots are excluded) **State Variable Analysis:** Introduction to state variable analysis: Concepts of state, state variable and state models. State model for Linear continuous –Time systems, solution of state equations. Text1: 8.1, 8.2, 8.4, 9.2, 9.3, 12.2, 12.3, 12.6	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Deduce transfer function of a given physical system, from differential equation representation or Block Diagram representation and SFG representation.
CO2	Calculate time response specifications and analyse the stability of the system.
CO3	Draw and analyse the effect of gain on system behaviour using root loci.
CO4	Perform frequency response Analysis and find the stability of the system.
CO5	Represent State model of the system and find the time response of the system.

Text Book	
1.	Control Systems Engineering, I J Nagrath, M. Gopal, New age international Publishers, 5th edition.

Reference text book	
1.	Modern control engineering, Katsuhiko Ogata, Person publishers, 5th edition
2.	Automatic control system, Benjamin. C. Kuo, Farid Golnaraghi, Wiley publishers, 8th Edition

Web links and Video lectures (e-Resources)
• https://nptel.ac.in/courses/108106098

LABORATORY

Practical Component of IPCC (12 Experiments)

Sl. No.	Name of the experimewnt
1.	Implement Block diagram reduction technique to obtain transfer function a control system.
2.	Implement Signal Flow graph to obtain transfer function a control system.
3.	Simulation of poles and zeros of a transfer function.
4.	Implement time response specification of a second order Under damped System, for different damping factors.
5.	Implement frequency response of a second order System.
6.	Implement frequency response of a lead lag compensator.
7.	Analyze the stability of the given system using Routh stability criterion.
8.	Analyze the stability of the given system using Root locus.
9.	Analyze the stability of the given system using Bode plots.
10.	Analyze the stability of the given system using Nyquist plot.
11.	Obtain the time response from state model of a system.
12.	Implement PI and PD Controllers.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

The CIE marks for the theory component of the Integrated Course (IC) shall be 30 marks and for the laboratory component 20 marks.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY COMPONENT OF IC:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes / Weekly test / project work for (20+20) marks, scaled down to **20 marks.**
4. Total marks scored **(30+20 = 50 marks)** scaled down to **25.**

CIE FOR THE PRACTICAL COMPONENT OF IC:

1. On completion of every experiment / program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day.
2. Each experiment is evaluated for 10 marks and scaled down to **5 marks.**
3. Laboratory test at the end of the 15th week of the semester / after completion of all the experiments shall be conducted for **50 marks** and scaled down to **20 marks.**
4. Total marks scored for lab component: **05+20=25 marks**.
5. The minimum marks to be secured in CIE to appear for SEE shall be 10(40% of maximum marks 25) in the theory and 10(40% of Maximum marks 25) in the practical.

6. The laboratory component of the **integrated course** shall be CIE only. However, in SEE, the questions from the practical component shall be included.

Theory				
IA Test	**Exam conducted for**	**Scaled down to**	**Average of best two tests**	**Total**
IA-1	**50**	**30**	**30**	**50/2=25**
IA-2	**50**	**30**		
IA-3	**50**	**30**		
Two Assignments	**2×10=20**	**10**	**10**	
Two Quizzes	**2×10=20**	**10**	**10**	

LAB			
Continuous performance and record writing	**Each experiments evaluated for 10 marks**	**Scaled down to 05 marks**	**5+20=25**
Internal Test + Viva voce	**Exam conducted for 50 marks**	**Scaled down to 20 marks**	

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and carries 20 Marks.
4. **Part-B** contains total 10 questions. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice. Students should answer five full questions, selecting one full question from each module.
5. Students have to answer for 100 marks and marks scored out of 100 shall be proportionally reduced to 50 marks.
6. The maximum marks from the practical component to be included in the SEE question paper is **16 marks.**
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	-	2	-	1	-	-	-	-	1	1
CO2	3	-	2	-	1	-	-	-	-	1	1
CO3	3	-	2	-	1	-	-	-	-	1	1
CO4	3	-	2	-	1	-	-	-	-	1	1
CO5	3	-	2	-	1	-	-	-	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-IV					
COMMUNICATION SYSTEM LAB –I **Category: PCCL**					
Course Code	:	B24EC405L	CIE	:	50 Marks
Teaching Hours L : T : P	:	0 : 0 : 2	SEE	:	50 Marks
Total Hours	:	15(P)	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Objectives	
1.	Understand the fundamental principles of analog communication systems, including concepts like amplitude modulation (AM), frequency modulation (FM), and phase modulation (PM).
2.	Design and test analog modulator and demodulator circuits, and to evaluate their performance in transmitting and receiving information.
3.	Design and implement analog pulse modulation such as PAM, PPM, PWM techniques.
4.	To demonstrate Multiplexing techniques like Time Division Multiplexing (TDM) in analog communication systems.
5.	To analyze the combination of multiple signals in Communication channels.

Sl. No	**List of Experiments**
1.	Amplitude Modulation and Demodulation of Standard AM
2.	Generation & Detection of DSBSC (LM741 and LF398 ICs can be used)
3.	Frequency Modulation using VCO and PLL FM Demodulation
4.	Pulse sampling, flat top sampling and reconstruction
5.	Pulse Amplitude Modulation and Demodulation
6.	Time Division Multiplexing and De-multiplexing of two band limited signals.
7.	Pre-Emphasis And De-Emphasis Circuits
8.	Design And Test BJT Mixer
9.	Pulse Width Modulation
10.	Pulse Position Modulation
11.	PLL Frequency Synthesizer
12.	Generation & Detection of PCM

Course Outcomes: At the end of the course, the students will be able to	
CO1	Demonstrate a strong understanding of the fundamental principles behind analog communication systems, modulation techniques like AM, FM, and PM.
CO2	Design and build analog modulator and demodulator circuits for AM, FM, and PM communication systems.
CO3	Acquire the skills to design and implement pulse modulation techniques like PAM, PPM, and PWM.
CO4	Demonstrate an understanding of multiplexing techniques, specifically Time Division Multiplexing (TDM), and its application in analog communication systems.
CO5	Apply their knowledge to efficiently combine multiple analog signals for transmission over shared communication channels.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

Component	Scale down to	Total Marks
Conduction of experiments and Record Writing (Each Experiment evaluated for 10 marks)	20	20
Internal Lab Test 1(After 6 experiments) Exam conduction for 50 marks	15	15
Internal Lab Test 2 (After 6 experiments) Exam conduction for 50 marks	15	15
	CIE	**50**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Students can pick one question (experiment) from the questions lot prepared by the examiners.
4. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
5. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
6. Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	1	1	3	3	-	-	-	2	2	2
CO2	3	1	1	3	2	-	-	-	3	2	2
CO3	3	1	1	3	3	-	-	-	2	2	2
CO4	3	1	1	3	2	-	-	-	2	2	2
CO5	3	1	1	3	2	-	-	-	2	2	2

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-IV					
MICROCONTROLLERS **Category: ESC/ETC/PLC-IV**					
Course Code	:	B24EC461	CIE	:	50 Marks
Teaching Hours/Week (L:T:P: S)	:	3:0:0	SEE	:	50 Marks
Total Hours	:	45 (T)	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Objectives	
1.	Understand the difference between Microprocessor and Microcontroller and embedded microcontrollers.
2.	Learn the basic architecture of 8051microcontroller.
3.	Learn to Program 8051 microcontroller using Assembly Language and C
4.	Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051
5.	Understand the interrupt structure of 8051 and Interfacing I/O devices using I/O ports of 8051.

Module – 1: Microcontroller	**No. of Hours**
Microprocessor Vs Microcontroller, Micro controller & Embedded Processors, Processor Architectures-Harvard Vs Princeton & RISC Vs CISC , 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing. (Text book 1-1.1,Text book 2-1.0,1.1,3.0,3.1,3.2,3.3)	9
Module – 2: Instruction Set	**No. of Hours**
Assembler Directives, 8051 Addressing Modes, Data Transfer Instructions, Arithmetic instructions, Logical Instructions, Jump & Call Instructions Stack & Subroutine Instructions of 8051 (with examples in assembly Language). (Text book 1-2.5,Text book 2- Chapter 5,6,7,8)	9
Module – 3: Timers/Counters & Serial port programming	**No. of Hours**
Basics of Timers & Counters, Data types & Time delay in the 8051 using C, Programming 8051 Timers, Mode 1 &Mode 2 Programming (Text book 2- 3.4, Text book 1- 7.1, 9.1) Basics of Serial Communication, 8051 Connection to RS232, Programming the 8051 to transfer data serially & to receive data serially using C.(Text book 2- 3.5, Text book 1- 10.1,10.2,10.3,10.5)	9
Module– 4: Interrupt Programming	**No. of Hours**
Basics of Interrupts, 8051 Interrupts, Programming Timer Interrupts, Programming Serial Communication Interrupts, Interrupt Priority in 8051(Assembly Language only) (Text book 2- 3.6, Text book 1- 11.1,11.2,11.4,11.5)	9
Module– 5: I/O Port Interfacing & Programming	**No. of Hours**
LCD interfacing, DAC 0808 Interfacing, ADC 0804 interfacing, Stepper motor interfacing, DC motor control & Pulse Width Modulation (PWM) using C only. (Text book 1- 12.1, 13.1, 13.2, 17.2, 17.3)	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Describe the difference between Microprocessor and Microcontroller, Types of Processor Architectures and Architecture of 8051Microcontroller.
CO2	Discuss the types of 8051 Microcontroller Addressing modes & Instructions with Assembly Language Programs.
CO3	Explain the programming operation of Timers/Counters and Serial port of 8051 Microcontroller.
CO4	Illustrate the Interrupt Structure of 8051 Microcontroller & its programming.
CO5	Develop C programs to interface I/O devices with 8051 Microcontroller.

Text Books	
1.	The “8051 Microcontroller and Embedded Systems – Using Assembly and C”, Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollind. Mckinlay; Phi, 2006 / Pearson, 2006.
2.	“The 8051 Microcontroller”, Kenneth j. Ayala, 3 rd edition, Thomson/Cengage Learning.

Reference Books	
1.	“The 8051 Microcontroller Based Embedded Systems”, Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.
2.	“Microcontrollers: Architecture, Programming, Interfacing and System Design”, Raj Kamal, Pearson Education, 2005.

Web links and Video lectures (e-Resources)
1. https://youtu.be/8MLV5GP7FMY?si=R5PW1AqINV4pO-JK
2 https://youtu.be/yYjPAhJ_YHM?si=C50l8qGBDlV5dSAu
3. https://youtu.be/2-geyR_aM28?si=QO3IvO3_i92DcgX8

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
5. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50).

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and it carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	-	3	2	3	-	-	-	-	1	1
CO2	3	-	3	2	3	-	-	-	-	1	1
CO3	3	-	3	2	3	-	-	-	-	1	1
CO4	3	-	3	2	3	-	-	-	-	1	1
CO5	3	-	3	2	3	-	-	-	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-IV					
EMBEDDED SYSTEMS AND IOT DESIGN **Category: ESC/ETC/PLC-IV**					
Course Code	:	B24EC462	CIE	:	50 Marks
Teaching Hours L : T : P	:	3:0:0	SEE	:	50 Marks
Total Hours	:	45(T)	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Objectives	
1.	Learn the architecture and features of 8051.
2.	Study the design process of an embedded system.
3.	Understand the real–time processing in an embedded system.
4.	Learn the architecture and design flow of IoT.
5.	Build an IoT based system.

Module – 1: 8051 Microcontroller	**No. of Hours**
Microcontrollers for an Embedded System – 8051 – Architecture – Addressing Modes – Instruction Set – Program and Data Memory – Stacks – Interrupts – Timers/Counters – Serial Ports – Programming.	9
Module – 2 : Embedded C Programming	**No. of Hours**
Memory And I/O Devices Interfacing – Programming Embedded Systems in C – Need For RTOS – Multiple Tasks and Processes – Context Switching – Priority Based Scheduling Policies.	9
Module – 3: Processes and Operating Systems	**No. of Hours**
Structure of a real – time system – Task Assignment and Scheduling – Multiple Tasks and Multiple Processes – Multirate Systems – Pre emptive real – time Operating systems – Priority based scheduling – Interprocess Communication Mechanisms – Distributed Embedded Systems – MPSoCs and Shared Memory Multiprocessors – Design Example – Audio Player, Engine Control Unit and Video Accelerator.	9
Module – 4: Iot Architecture and Protocols	**No. of Hours**
Internet – of – Things – Physical Design, Logical Design – IoT Enabling Technologies – Domain Specific IoTs – IoT and M2M – IoT System Management with NETCONF – YANG – IoT Platform Design – Methodology – IoT Reference Model – Domain Model – Communication Model – IoT Reference Architecture – IoT Protocols – MQTT, XMPP, Modbus, CANBUS and BACNet.	9
Module – 5: Iot System Design	**No. of Hours**
Basic building blocks of an IoT device – Raspberry Pi – Board – Linux on Raspberry Pi – Interfaces – Programming with Python – Case Studies: Home Automation, Smart Cities, Environment and Agriculture.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Explain the architecture and features of 8051
CO2	Develop a model of an embedded system.
CO3	List the concepts of real time operating systems.
CO4	Learn the architecture and protocols of IoT.
CO5	Design an IoT based system for any application.

Text Books	
1.	Mohammed Ali Mazidi, Janice GillispieMazidi, RolinD.McKinlay, The 8051 Microcontroller and Embedded Systems Using Assembly and C, Second Edition, Pearson Education, 2008.(Unit – I)
2.	Marilyn Wolf, Computers as Components – Principles of Embedded Computing System Design, Third Edition, Morgan Kaufmann, 2012.(Unit – II,III)
3.	ArshdeepBahga, Vijay Madisetti, Internet – of- Things – A Hands on Approach, Universities Press, 2015.(Unit – IV,V)

REFERENCE BOOKS	
1.	MayurRamgir, Internet – of – Things, Architecture, Implementation and Security, First Edition, Pearson Education, 2020.
2.	LylaB.Das, Embedded Systems: An Integrated Approach, Pearson Education 2013.
3.	Jane.W.S .Liu, Real – Time Systems, Pearson Education, 2003.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
5. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50).

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and it carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
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CO2	3	3	3	2	2	2	-	-	-	-	1
CO3	3	3	2	2	2	1	-	-	-	-	1
CO4	3	3	2	2	2	2	-	-	-	-	1
CO5	3	3	3	3	3	1	-	-	-	-	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-IV					
SMART SENSORS **Category: ESC/ETC/PLC-IV**					
Course Code	:	B24EC463	CIE	:	50 Marks
Teaching Hours L : T : P	:	3:0:0	SEE	:	50 Marks
Total Hours	:	45(T)	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Objectives	
1.	Learn the basics of smart sensors and overview of smart sensing.
2.	Realizing the interfacing of MCUs and DSPs for sensors
3.	Study of sensor communication and MEMS
4.	Study the testing & reliability of sensors.
5.	Learn the concept of smart sensors in real world.

Module – 1: Basics of Smart Sensors & Micromachining	**No. of Hours**
Introduction, Mechanical-Electronic transitions in sensing, nature of sensors, overview of smart sensing and control systems, integration of micromachining and microelectronics, introduction to micromachining, bulk micromachining, wafer bonding, surface micromachining, other micromachining techniques.	9
Module – 2 : Sensor Information To MCU	**No. of Hours**
Introduction, amplification and signal conditioning, separate versus integrated signal conditioning, digital conversion. MCUs and DSPs for sensor : Introduction, MCU control, MCUs for sensor interface, DSP control, Software, tools and support, sensor integration.	9
Module – 3: Communications for Smart Sensors	**No. of Hours**
Introduction, definitions and background, sources and standards, automotive protocols, industrial networks, office & building automation, home automation, protocols in silicon, other aspects of network communications. Sensor Communication and MEMS :Wireless zone sensing, surface acoustical wave devices, intelligent transportation system, RF-ID, Micro optics, micro-grippers, micro-probes, micro- mirrors, FEDs, communications for smart sensors - sources and standards, automotive protocols, industrial networks, office and building automation, home automation, protocols in silicon, other aspects of network communications.	9
Module – 4: Packaging, Testing and Reliability of Smart Sensors	**No. of Hours**
Introduction, Semiconductor packaging applied to sensors, hybrid packaging, packaging for monolithic sensors, reliability implications, testing smart sensors. Unit Standards for Smart Sensors: Introduction, setting the standards for smart sensors and systems, IEEE 1451.1, IEEE 1451.2, IEEE P1451.3, IEEE 1451.4, extending the systems to network.	9
Module – 5: Implications of Smart Sensor Standards and Recent Trends	**No. of Hours**
Introduction, sensor plug-and-play, communicating sensor data via existing wiring, automated/remote sensing and web, process control over the internet, alternative standards, HVAC sensor chip, MCU with integrated pressure sensors, alternative views of smart sensing, smart loop.	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Understand the principle of smart sensors and process in development of smart sensors.
CO2	Develop intelligent systems by interfacing the smart sensors to MCUs and DSPs.
CO3	Analyze the use of smart sensors in communication, MEMS and automation.
CO4	Evaluate the standards of smart sensors by the assessment of reliability testing and packaging.
CO5	Analyze the applications of smart sensors in different fields and recent development

Text Books	
1.	Understanding Smart Sensors- Randy Frank, 2nd Edition. Artech House Publications, 2013.
Reference Text Books	
1.	G. K. Ananthasuresh, K. J. Vinoy, S. Gopalakrishnan, K. N. Bhat, V. K. Aatre, Micro and Smart Systems: Technology and modeling, Willey Publications,2012.

Web links and Video lectures (e-Resources)
1.https://nptel.ac.in/courses/122106025 2. https://nptel.ac.in/courses/108105132 3. https://nptel.ac.in/courses/117104072

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of continuous Internal Evaluation (CIE) is 50% and for the Semester End Examination (SEE) is 50%. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50). The minimum passing mark for SEE is 35% of maximum marks (18 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. Student has to secure a minimum 40% (40 marks out of 100) in the total of the CIE and SEE together.

CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
5. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50).

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and it carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	-	-	-	-	3	1	-	-	1	2
CO2	2	-	-	-	-	2	1	-	-	2	2
CO3	1	-	-	-	-	1	2	-	-	2	1
CO4	1	-	-	-	-	1	2	-	-	1	1
CO5	1	-	-	-	-	1	2	-	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER - IV					
JAVA PROGRAMMING **Category: ESC/ETC/PLC-IV** **(Common to ECE, EEE, RA)**					
Course Code	:	B24EC464	CIE	:	50 Marks
Teaching Hours L:T : P	:	3:0:0	SEE	:	50 Marks
Total Hours	:	45(T)	Total	:	100 Marks
Credits	:	3	SEE Duration	:	3 Hrs

Course Objectives	
1.	To learn primitive constructs JAVA programming language.
2.	To understand Object Oriented Programming Features of JAVA.
3.	To gain knowledge on packages, multithreaded programming and exceptions.

Module–1: An Overview of Java	**No. of Hours**
Object-Oriented Programming (Two Paradigms, Abstraction, The Three OOP Principles), Using Blocks of Code, Lexical Issues (Whitespace, Identifiers, Literals, Comments, Separators, The Java Keywords). **Data Types, Variables, and Arrays:** The Primitive Types (Integers, Floating-Point Types, Characters, Booleans), Variables, Type Conversion and Casting, Automatic Type Promotion in Expressions, Arrays, Introducing Type Inference with Local Variables. **Operators:** Arithmetic Operators, Relational Operators, Boolean Logical Operators, The Assignment Operator, The Operator, Operator Precedence, Using Parentheses. **ControlStatements:**Java'sSelectionStatements(if,TheTraditionalswitch),Iteration Statements (while, do-while, for, The For-Each Version of the for Loop, Local Variable Type Inference in a for Loop, Nested Loops), Jump Statements (Using break, Using continue, return).	9
Module–2: Introducing Classes	**No. of Hours**
Class Fundamentals**,** Declaring Objects**,** Assigning Object Reference Variables**,** Introducing Methods, Constructors**,** The this Keyword**,** Garbage Collection. **Methods and Classes:** Overloading Methods, Objects as Parameters, Argument Passing, Returning Objects, Recursion, Access Control, Understanding static, Introducing final, Introducing Nested and Inner Classes.	9
Module–3: Inheritance and Interfaces	**No. of Hours**
Inheritance: Inheritance Basics, Using super, Creating a Multilevel Hierarchy, When Constructors Are Executed, Method Overriding, Dynamic Method Dispatch, Using Abstract Classes, Using final with Inheritance, Local Variable Type Inference and Inheritance, The Object Class. **Interfaces:** Interfaces, Default Interface Methods, Use static Methods in an Interface, Private Interface Methods.	9
Module–4: Packages and Exceptions	**No. of Hours**
Packages: Packages, Packages and Member Access, Importing Packages. **Exceptions:**Exception-HandlingFundamentals**,**ExceptionTypes**,**UncaughtExceptions**,**Using try and catch, Multiple catch Clauses, Nested try Statements, throw, throws, finally, Java's Built- in Exceptions, Creating Your Own Exception Subclasses, Chained Exceptions.	9
Module–5: Multithreaded Programming	**No. of Hours**
Multithreaded Programming: The Java Thread Model, The Main Thread, Creating a Thread, Creating Multiple Threads, Using is Alive() and join(), Thread Priorities, Synchronization, Interthread Communication, Suspending, Resuming, and Stopping Threads, Obtaining a Thread's State. **Enumerations, Type Wrappers and Autoboxing:** Enumerations (Enumeration Fundamentals**,** The values() and value Of() Methods), Type Wrappers (Character, Boolean, The Numeric Type Wrappers),Autoboxing(AutoboxingandMethods,Autoboxing/UnboxingOccursinExpressions, Autoboxing /Unboxing Boolean and Character Values).	9

Course Outcomes: At the end of the course, the students will be able to	
CO1	Demonstrate proficiency in writing simple programs involving branching and looping structures.
CO2	Design a class involving data members and methods for the given scenario.

CO3	Apply the concepts of inheritance and inter faces in solving real world problems.
CO4	Use the concept of packages and exception handling in solving complex problem.
CO5	Apply concepts of multi threading, autoboxing and enumerations in program development

Text Books	
1.	HerbertSchildt,JavaTheCompleteReference,7thEdition,TataMcGrawHill, 2007.

Reference Text Books	
1.	MaheshBhaveandSunilPatekar,"ProgrammingwithJava",FirstEdition,PearsonEducation,2008, ISBN:9788131720806
2.	RajkumarBuyya,SThamarasiselvi,xingchenchu,ObjectorientedProgrammingwithjava,TataMcGraw Hill education private limited
3.	EBalagurusamy,ProgrammingwithJavaAprimer,TataMcGrawHill companies
4.	AnitaSethandBLJuneja,JAVAOnestepAhead,OxfordUniversityPress,2017

Web links and Video lectures (e-Resources)	
1.	JavaTutorial:https://www.geeksforgeeks.org/java/
2.	Introduction To Programming In Java (by Evan Jones, Adam Marcus and Eugene Wu):https://ocw.mit.edu/courses/6-092-introduction-to-programming-in-java-january-iap-2010/
3.	JavaTutorial:https://www.w3schools.com/java/
4.	JavaTutorial:https://www.javatpoint.com/java-tutorial

ASSESSMENT DETAILS BOTH (CIE AND SEE)

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CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

1. Three tests each of 50 marks, after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
5. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50).

SEMESTER END EXAMINATION (SEE)

1. The question paper shall be set for 100 marks and duration of SEE is 3 hours.
2. The question paper will have two parts: Part-A and Part-B.
3. **Part-A** should contain minimum **Two or Four** quiz questions from each module of 02 marks/ 01 marks each. **Part-A is Compulsory** and it carries 20 Marks.
4. **Part-B** contains total 10 questions.
5. Two questions of 16 marks (with minimum of 3 sub questions) from each module with internal choice.
6. Students should answer five full questions, selecting one full question from each module.
7. Question papers to be set as per the Blooms Taxonomy levels.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	-	1	2	2	1	1	-	1	2	1
CO2	1	-	1	2	2	-	-	-	1	1	1
CO3	2	-	1	2	3	-	-	-	1	1	1
CO4	2	-	1	1	1	1	1	-	1	2	1
CO5	1	-	1	2	2	1	1	-	2	1	1

Level3 -High, Level2- Moderate, Level1- Low

SEMESTER- IV					
PROGRAMMABLE LOGIC CONTROLLERS **Category: AEC/SEC-I** **(Common to ECE, RA)**					
Course Code	:	B24EC481	CIE	:	50 Marks
Teaching Hours L : T : P	:	1:0:0	SEE	:	50 Marks
Total Hours	:	15(T)	Total	:	100 Marks
Credits	:	1	SEE Duration	:	1 Hr

Course Objectives	
1.	To understand the need for automation in the industry with basic controller mechanisms involved.
2.	To study programming concepts to achieve the desired goal or to define the various steps involved in the automation.
3.	To understand programming involved with basic subroutine functions.
4.	To make use of the internal hardware circuits of automation circuit to control the devices during various states by monitoring the timers and counters.
5.	To handle the data of the I/O devices to interface the data with the controller and auxiliary devices.

Module – 1: Introduction	**No. of Hours**
Programmable logic controller (PLC), role in automation (SCADA), advantages and disadvantages, hardware, internal architecture, sourcing and sinking (Textbook 1: 1.1 to 1.4) I/O devices and Processing: list of input and output devices, examples of applications. I/O processing, input/output units, signal conditioning, remote connections, networks, processing inputs I/O addresses. (TextBook1: 2.1 to 2.3 and 4.1 to 4.7).	3
Module – 2 : Programming	**No. of Hours**
Ladder programming- ladder diagrams, logic functions, latching, multiple outputs, entering programs, functional blocks, program examples like location of stop and emergency switches. (TextBook1: 5.1 to 5.7).	3
Module – 3: Programming Methods	**No. of Hours**
Instruction Lists- Ladder programs and Instruction lists, Branch codes, Programming Examples- Signal lamp-valve operation task. Sequential Function Charts- Branching and convergence. (TextBook1: 6.1 to 6.3).	3
Module – 4: Internal Relays	**No. of Hours**
ladder programs, battery-backed relays, one-shot operation, set and reset, master control relay (TextBook1: 7.1 to 7.6). Timers and counters: Types of timers, ON and OFF- delay timers, pulse timers, forms of counter, programming, up and down counters. (TexBook1: 9.1 to 9.6).	3
Module – 5: Shift register and data handling	**No. of Hours**
Shift registers, ladder programs, registers and bits, data handling, arithmetic functions. (TextBook1: 11.1 to 11.2 and 12.1 to 12.3)	3

Course Outcomes: At the end of the course, the students will be able to	
CO1	Understand the PLC and how to construct PLC ladder diagrams.
CO2	Demonstrate an application with programming.
CO3	Analyze the characteristics of registers and conversion examples.
CO4	Apply PLC functions to timing and counting applications.
CO5	Analyse the analog operation of PLC and demonstrate the robot applications with PLC.

Text Books	
1.	Programmable Logic controllers-W Bolton, 5th edition/6th edition, Elsevier- newness, 2009/2015.
2.	Programmable logic controllers - principles and applications"-John W. Webb, Ronald A Reiss, Pearson education, 5th edition, 2007.
Reference Text Books	
1.	Programmable Logic Controllers"- E. A Paar, 3rd Edition, An Engineers Guide. Newness, 2003.
2.	"Introduction to Programmable Logic Controller"- Garry Dunning, 3rd Edition, Thomson Asia Pte Ltd. Publication, 2006

Web links and Video lectures (e-Resources)
1.https://nptel.ac.in/courses/122106025 2. https://nptel.ac.in/courses/108105132 3. https://nptel.ac.in/courses/117104072

ASSESSMENT DETAILS (BOTH CIE AND SEE)

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CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

1. Three tests each of 50 marks (Multiple Choice Questions), after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
5. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50).

SEMESTER END EXAMINATION (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is 01 hour. The student has to secure a minimum of 35% of the maximum marks meant for SEE.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	1	-	1	1	-	-	-	-	1	2
CO2	2	2	-	1	1	-	-	-	-	2	2
CO3	1	1	-	1	1	-	-	-	-	2	1
CO4	1	1	-	1	1	-	-	-	-	1	1
CO5	1	1	-	1	1	-	-	-	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER- IV					
INTRODUCTION TO ARTIFICIAL INTELLIGENCE **Category: AEC/SEC-IV**					
Course Code	:	B24EC482	CIE	:	50 Marks
Teaching Hours L : T : P	:	1 : 0 : 0	SEE	:	50 Marks
Total Hours	:	15(T)	Total	:	100 Marks
Credits	:	1	SEE Duration	:	1Hrs

Course Objectives	
1.	To impart artificial intelligence principles, techniques, and history.
2.	To assess the applicability, strengths, and weaknesses of the basic knowledge representation,problem- solving, and learning methods in solving engineering problems.
3.	To develop intelligent systems by assembling solutions to concrete computational problems

Module – 1: Artificial Intelligence	**No. of Hours**
Introduction to AI, foundations of AI, History of AI, state of the art, Intelligent agents, agents and environments. Nature of the environment, structure of agent Text1: 1.1 – 1.4, 2.1, 2.3, 2.4	5
Module – 2: Problem Solving	**No. of Hours**
Problem-solving by Searching : problem solving agents, example problems, searching for solutions, uniform search strategies Text1 : 3.1 – 3.4	5
Module – 3: Adverserial search	**No. of Hours**
Games, optimal decisions in games, alpha beta pruning, imperfect real time decisions, stochastic games. Text1: 5.1 – 5.5	6
Module – 4: knowledge Reasoning	**No. of Hours**
Knowledge based agents, the WUMPUS world, logic, propositional logic, propositional theorem proving, effective propositional model checking. Text1 : 7.1 – 7.6	6
Module – 5: Learning Systems	**No. of Hours**
supervised learning, learning decision tree, Regression and classification with linear models, artificial neural network, non parametric model, support vector machines Text1 : 18.2, 18.3, 18.6 – 18.9	6

Course Outcomes: At the end of the course, the students will be able to	
CO1	Evaluate Artificial Intelligence(AI) methods and describe their foundations.
CO2	Apply basic principles of AI in solutions that require problem-solving, inference, perception, knowledge representation, and learning.
CO3	Demonstrate knowledge of reasoning and knowledge representation for solving real-world problems
CO4	Analyze and illustrate how search algorithms play vitalrole in problem solving
CO5	llustrate the construction of learning, expert system, the current scope and limitations of AI.

Text Books	
1.	Russell, S and Norvig, P. 2015. Artificial Intelligence-A Modern Approach,3rd edition, Prentice-Hall.
2.	Poole, D and Mackworth, A. 2010. Artificial Intelligence: Foundations of Computational Agents, Cambridge University Press.
Reference Text Books	
1.	Ric, E., Knight, Kand Shankar, B.2009. Artificial Intelligence, 3rd edition, Tata McGraw Hill.
2.	Design of Machinery Robert L.Norton, McGraw Hill 2001
3.	Luger, G.F. 2008. Artificial Intelligence Structures and Strategies for Complex Problem Solving, 6th edition, Pearson.
4.	Brachman, R. and Levesque,H .2004. Knowledge Representation and Reasoning, Morgan

	Kaufmann.

Web links and Video lectures (e-Resources)
https://youtu.be/ZqfCqOpr2Ds?si=KRINFc5M1-YphhVv https://youtu.be/AETGmGYy0UU?si=iL1wodkTHjCrKjJT https://archive.nptel.ac.in/content/storage2/courses/106105078/pdf/Lesson%2001.pdf https://www.youtube.com/watch?v=wnqkfpCpK1g https://pll.harvard.edu/course/cs50s-introduction-artificial-intelligence-python https://azure.microsoft.com/en-us/resources/cloud-computing-dictionary/artificial-intelligencevs-machine-learning https://youtu.be/t4K6lney7Zw https://www.youtube.com/watch?v=QDX-1M5Nj7s

ASSESSMENT DETAILS (BOTH CIE AND SEE)

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CONTINUOUS INTERNAL EVALUATION (CIE)

CIE FOR THE THEORY:

1. Three tests each of 50 marks (Multiple Choice Questions), after the completion of the syllabus 40%, 70% and 100% respectively.
2. Average of best two internal assessment tests each of 50 marks, scale down to 30 marks.
3. Any two assessment methods as per regulations i.e. Two assignments / Two Quizzes/ Weekly test / project work for 40 marks, scaled down to 20 marks.
4. Total marks scored (30+20 = 50 marks).
5. The minimum passing mark for the CIE is 40% of maximum marks (20 marks out of 50).

SEMESTER END EXAMINATION (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is 01 hour. The student has to secure a minimum of 35% of the maximum marks meant for SEE.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	1	1	1	1	-	-	-	-	1	1
CO2	2	1	1	1	1	-	-	-	-	1	1
CO3	2	1	1	1	1	-	-	-	-	1	1
CO4	2	1	1	1	1	-	-	-	-	1	1
CO5	2	1	1	1	1	-	-	-	-	1	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER-IV					
MICROCONTROLLERS LABORATORY **Category: AEC/SEC-IV**					
Course Code	:	B24EC483	CIE	:	50 Marks
Teaching Hours L : T : P	:	0 : 0 : 2	SEE	:	50 Marks
Total Hours	:	15(P)	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Objectives	
1.	Grasp the fundamental concepts of microcontrollers and explore their practical applications.
2.	Develop a strong understanding of 8051 microcontroller architecture and gain hands-on experience with assembly language programming.
3.	Implement device control and automation using ALP/ C programming techniques.
4.	Learn the principles and methods of input/output (I/O) interfacing for building real-time embedded system applications.

Sl. No	**List of Experiments**
	PROGRAMMING
1.	Data Transfer - Block move, Exchange, Sorting, Finding largest element in an array.
2.	Arithmetic Instructions - Addition/subtraction, multiplication and division, square, Cube(Bit manipulations).
3.	Counters.
4.	Boolean & Logical Instructions (Bit manipulations).
5.	Conditional CALL & RETURN.
6.	Code conversion
7.	Programs to generate delay. Programs using serial port and on-Chip timer /Counter.
	INTERFACING Write ALP/C programs to interface 8051 chip to Interfacing modules to develop single chip solutions.
8.	Stepper and DC motor control interface to 8051.
9.	Generate different waveforms Sine, Square, Triangular, Ramp etc. using DAC interface to 8051; change the frequency and amplitude.
10.	External ADC and Temperature control interface to 8051.
11.	Alphanumeric LCD panel and Hex keypad input interface to 8051.
12.	Write a C program to (i) transmit and (ii) to receive a set of characters serially by interfacing 8051 to a terminal

Course Outcomes: At the end of the course, the students will be able to	
CO1	Enhance foundational programming abilities by applying *Assembly language* and *C* in microcontroller-based environments.
CO2	Write and analyze 8051 *Assembly language programs* to solve basic computational problems involving input data manipulation using a variety of instructions.
CO3	Interface and control peripheral input/output devices with the 8051 microcontroller through Assembly programming.
CO4	Demonstrate serial communication by interfacing serial devices with the 8051 and implementing data transfer using *C programming*.
CO5	Design and develop real-time embedded applications using the 8051 microcontroller.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

Component	Scale down to	Total Marks
Conduction of experiments and Record Writing (Each Experiment evaluated for 10 marks)	20	20
Internal Lab Test 1(After 6 experiments) Exam conduction for 50 marks	15	15
Internal Lab Test 2 (After 6 experiments) Exam conduction for 50 marks	15	15
	CIE	**50**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Students can pick one question (experiment) from the questions lot prepared by the examiners.
4. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
5. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
6. Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	2	1	3	-	3	-	-	-	-	-	1
CO2	2	1	3	-	3	-	-	-	-	-	1
CO3	2	1	3	-	3	-	-	-	-	-	1
CO4	2	1	3	-	3	-	-	-	-	-	1
CO5	2	1	3	-	3	-	-	-	-	-	1

Level 3 - High, Level 2 - Moderate, Level 1 - Low

SEMESTER - IV					
ARDUINO AND RASPBERRY PI LAB **Category: AEC/SEC-IV** **(Common to ECE, EEE, RA)**					
Course Code	:	B24EC484	CIE	:	50 Marks
Teaching Hours L : T : P	:	0 : 0 : 2	SEE	:	50 Marks
Total Hours	:	15(P)	Total	:	100 Marks
Credits	:	1	SEE Duration	:	3 Hrs

Course Objectives	
1.	To understand interfacing of basic I/O devices (LEDs, buzzers, buttons) with Arduino/Raspberry Pi.
2.	To understand sensor interfacing (temperature, humidity, current, distance, analog sensors) and data acquisition.
3.	To understand actuator control using relays, motors, and real-time clock integration.
4.	To apply the cocept of wireless communication and IoT connectivity using Bluetooth and cloud platforms.
5.	To comprehend skills for measuring, monitoring, and transmitting energy-related parameters for smart applications

Sl. No	**List of Experiments** **PROGRAMMING**
1.	i) To interface LED/Buzzer with Arduino and write a program to ‘turn ON’ LED for 1 sec after every 2 seconds. ii) ii) To interface Push button/Digital sensor (IR/LDR) with Arduino and write a program to ‘turn ON’ LED when push button is pressed or at sensor detection.
2.	i) To interface DHT11 sensor with Arduino and write a program to print temperature and humidity readings. ii) ii) To interface OLED with Arduino and write a program to print temperature and humidity readings on it.
3.	To interface motor using relay with Arduino and write a program to ‘turn ON’ motor when push button is pressed.
4.	To interface Bluetooth with Arduino and write a program to send sensor data to Smartphone using Bluetooth.
5.	To interface Bluetooth with Arduino and write a program to turn LED ON/OFF when '1'/'0' is received from Smartphone using Bluetooth.
6.	Write a program to interface an analog sensor (e.g., potentiometer or temperature sensor) with Arduino and display the analog values on the Serial Monitor.
7.	To interface a Real-Time Clock (DS3231/DS1307) module with Arduino and write a program to display the current date and time on the Serial Monitor.
8.	Write a program to measure an analog voltage (0–5V) using Arduino and display the measured voltage on the Serial Monitor.
9.	Interface a current sensor (e.g., ACS712) with Arduino and write a program to measure and display the current flowing through a load on the Serial Monitor.
10.	To interface a DC motor through a relay module with Arduino/ Raspberry Pi and write a Python program to turn ON the motor when a push button is pressed.
11.	Interface an ultrasonic sensor (HC-SR04) with Arduino/ Raspberry Pi and write a program to measure and

	display the distance in centimeters on the Serial Monitor.
12.	Write a python program on Raspberry Pi to upload temperature and humidity data to thing speak cloud.

Course Outcomes: At the end of the course, the students will be able to	
CO1	Understand the interfacing and control of digital devices such as LEDs and buzzers using Arduino.
CO2	Understand sensor interface to acquire and display data from temperature, humidity, distance, voltage, and current sensors.
CO3	Design motor and relay-based actuation systems using sensor input for automation and control.
CO4	Analyze communication techniques for exchanging data with smartphones and cloud servers using Bluetooth and IoT.
CO5	Understand and evaluate methods for measuring and transmitting sensor parameters using Raspberry Pi.

ASSESSMENT DETAILS BOTH (CIE AND SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CONTINUOUS INTERNAL EVALUATION (CIE)

Component	Scale down to	Total Marks
Conduction of experiments and Record Writing (Each Experiment evaluated for 10 marks)	20	20
Internal Lab Test 1(After 6 experiments) Exam conduction for 50 marks	15	15
Internal Lab Test 2 (After 6 experiments) Exam conduction for 50 marks	15	15
	CIE	**50**

SEMESTER END EXAMINATION (SEE)

1. SEE marks for the practical course are 50 Marks. Practical examinations are to be conducted between the schedules mentioned in the academic calendar of the Institution.
2. All laboratory experiments are to be included for practical examination.
3. Students can pick one question (experiment) from the questions lot prepared by the examiners.
4. Evaluation of test write-up, conduction procedure, result and viva will be conducted jointly by examiners.
5. Rubrics suggested for SEE, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks.
6. Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero. The minimum duration of SEE is 03 hours.

CO-PO Mapping

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	-	-	2	-	-	-	-	-	2
CO2	3	2	-	2	3	-	-	-	-	-	2
CO3	3	3	3	2	3	-	-	-	1	1	2
CO4	3	3	2	2	3	1	-	-	2	2	2
CO5	3	3	2	2	3	2	2	1	2	2	3

Level-1-High, Level-2-Moderate, Level-3-Low