



Webinar On “VLSI – Standard Cell Design”

- **Date:** 24th May 2020
- **Resource Person:** Mr. G. Prashanth Reddy Team lead, Intel India, Bangalore
- **Platform:** Zoom Meeting, ID: 87541324699
- **Objective :**
 - To enlighten the students with basic VLSI Standard Cell Design
 - To provide a better understanding of Cell Design & Issues related as per the need of industry
- **No. of participants:** 113
- **Target Participants:** Students of 4th and 6th semester of ECE department.
- **Outcome of the event:** The Students gained knowledge on
 - Basics of VLSI & Cell Designs.
 - Timing Analysis of Memory Cells, Latency, Pipelining.
 - Obtained a practical exposure on VLSI Design.
 - Various Job Opportunities VLSI Industries.

Webinar

On

"VLSI – Standard Cell Design"

RAJARAJESWARI COLLEGE OF ENGINEERING

CET CODE: E145 COMED-K: E099

DEPT. OF ELECTRONICS & COMMUNICATION ENGINEERING

Webinar on "VLSI- A Standard Cell Design"

FREE REGISTRATION

Registration Link: <https://forms.gle/ID9y3xah7jGzQZ8>

E-certificates will be provided

Admissions Open 2020

Mr. Prashanth Reddy,
Functional Safety Architect,
Intel India Pvt Ltd,
Bangalore

DATE: 24 MAY 2020
TIME: 11 AM TO 12:30 PM

Get Connected with us
Zoom ID: 87541324699
Password: 708041

Standard cell Design

Gadila Prashanth Reddy

About Author

Gadila Prashanth Reddy

15+ Years experience in Intel India PVT Ltd

Job Roles

- Standard cell design
- ICN design engineer - PCB
- PMIC electrical validation Engineer
- ASIC architecture - Functional Safety

Research Scholar (Ph.D.) & Teaching

Guest Lectures: VIT university, RREC Bangalore, SVEC Nellore, SREC Anantapur, TRR Hyderabad, True VLSI, Sayarbh Embedded systems, Gunturpeti Nellore and Free transporter engineering Articles

Patents & Publications

International Patent Submissions

- "An Apparatus for Detection of Gas Leakage", India Patent number 201941003789, Publication number : 201941003789
- "Single Chip Multi-Die Architecture Having Cross-Monitoring Capability" - Publication number : 20190294125

International Journal and Conference publications

Title: *Estimation of Failure Rate of Bulk Voltage Regulator*, Publication: Published as a article in Journal - IJRTTE (International Journal of recent Technology and engineering) in Volume 9, Issue 258 | link : <https://www.ijrtte.org/issue/volume-9-issue-258/>

Title: *Matrix Approach to Perform Dependent Failure Analysis in Compliance with Functional Safety Standards*, Publications: Published in Springer proceedings in 3rd International Conference on Computational Intelligence and Informatics (ICCI-2019), Link: <http://www.springer.com/book/9789815547214>

Title: *Assessing Functional Safety Parameters with respect to safety application*, Publication: "International Journal of Advance Science and Technology" received acceptance and publication in process

Title: *"Achieving ISO 26262 IEC 61508 objectives with a common development process"*, Publication : Published in Taylor and Francis conference proceedings in

Today's Topic

11:04 AM 7.4KB/s 4G+ 50

Close Participants (59)

Search

	Sumitha Manoj (me)			>
	SelectSmart ops (host)			>
	ranga R (co-host)			>
	Daphne (co-host)			>
	Prashanth Reddy (co-host)			>
	selectsmart ops (co-host)			>
	10-C KIRTHANA			>
	admin			>
	Ambika M S			>
	Amogh K-1RR16TE002			>

Invite

HOD/ECE

